

# Model Name: G1.Sniper B5

1.1

SHEET

TITLE

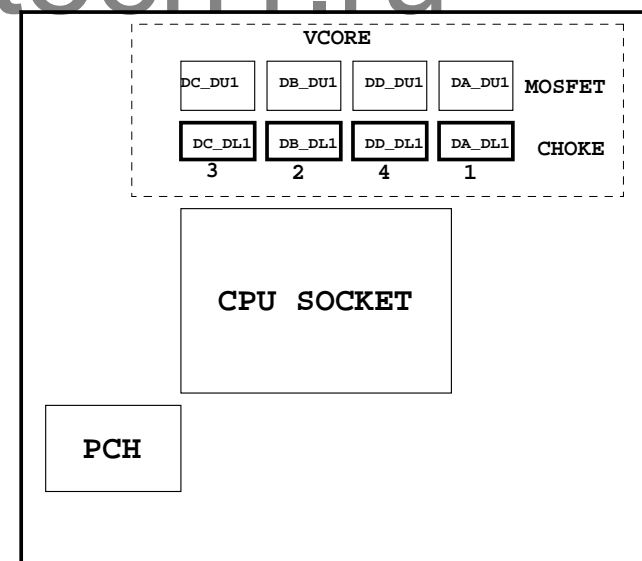
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS / LPT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE_ ISL95820_1
24	VCORE_ ISL95820_2
25	DDR15V / M3 POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET

TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	Realtek 8111F-VL
32	DVI
33	HDMI
34	TABLE LIST
35	
36	
37	
38	
39	
40	

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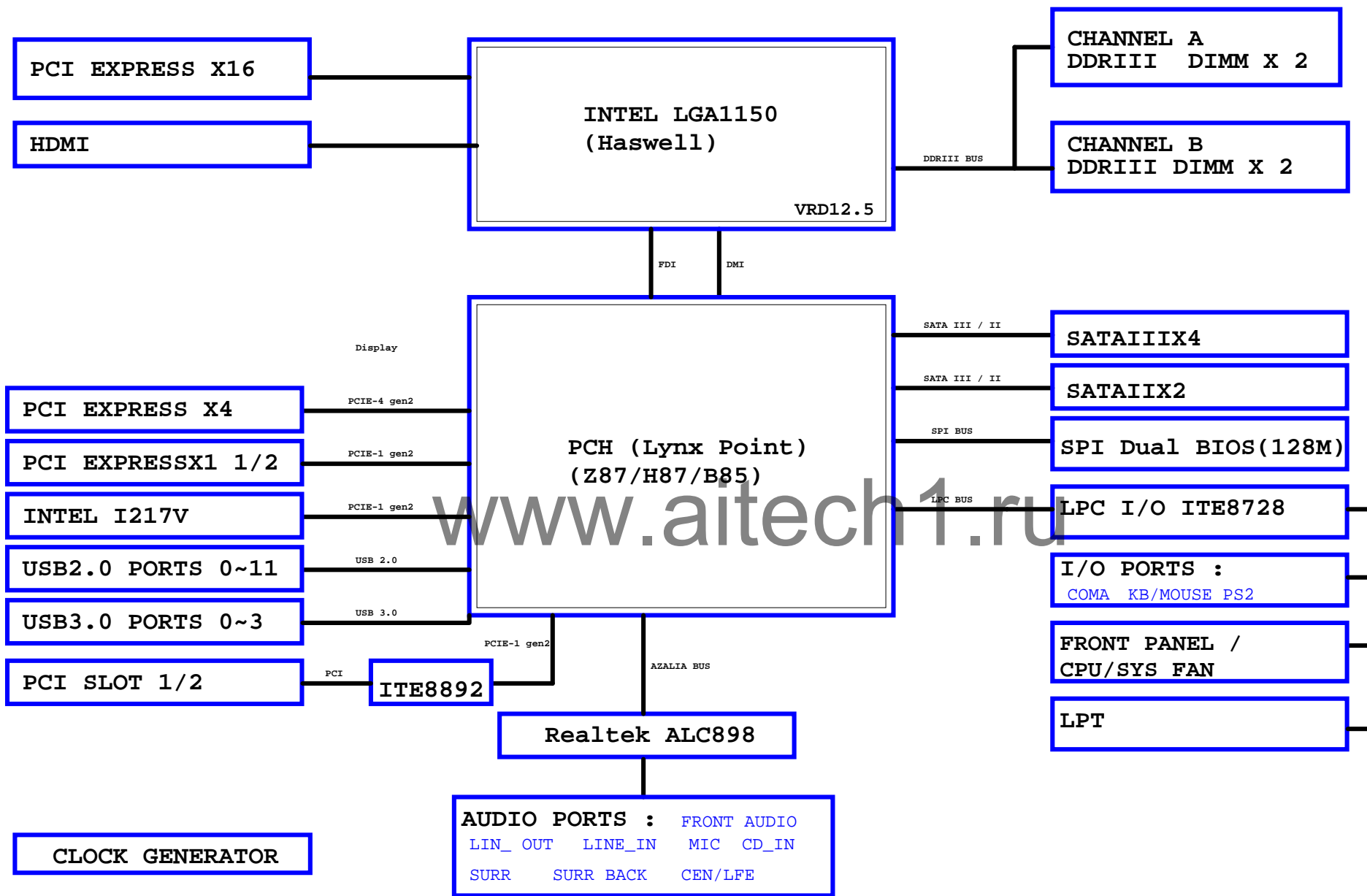


## Component value change history

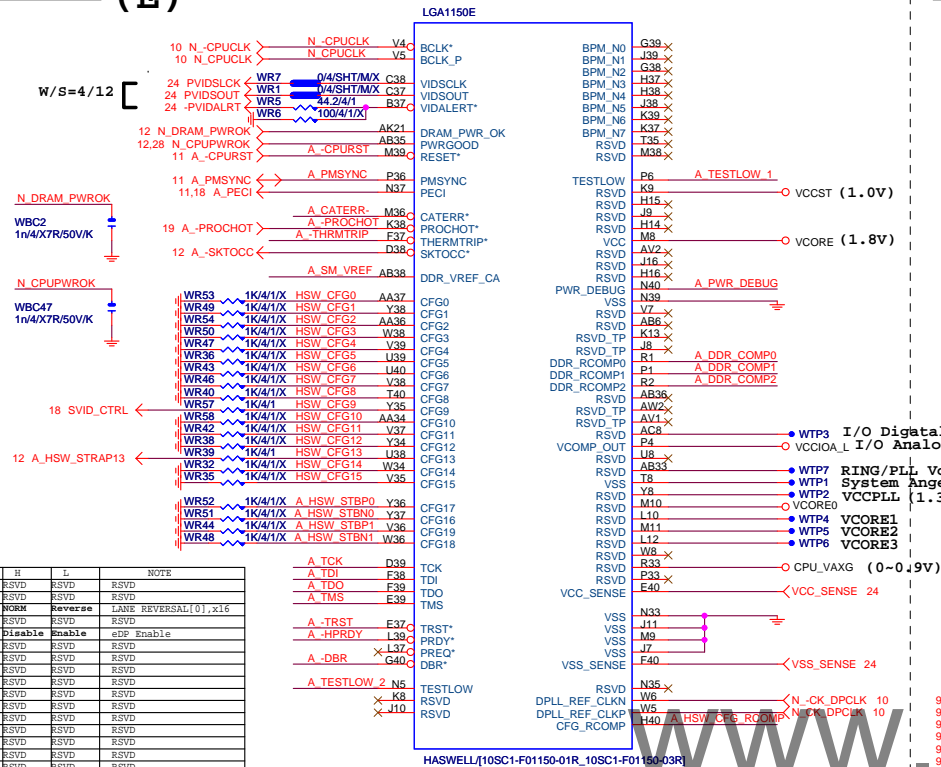
[illegible]

DATE	Change Item	Reason
0.1	1. B85-HD3 Rev0.2修改 1. LAN --> I2L7 , AUDIO --> ALC898 0. Remove USB ESDIC "UAR1,UBR1" power 1ohm 1. 0 ohm --> short pad 2. 简化CPU Config setting 3. 背板电容移除或mask (包含pch) 4. Remove BIOS "CS" pin 5. UBF9/UBF10 1206 --> 0805 6. N_GPIO37 pull-up to VCC3 7. +12V RN2-RN6要不要上? Add VCC/VCC3/5VSB dummy load 8. 5VSB/5VDUAL OVP protection 9. 预留N_PCH_DPWROK 控制线路 10. USB2.0 port2/3 , 4/5 swap	
0.2	1. AUDIO AGND LED切割线(COMP/SOLDER要挖空) 2. Update AUDIO_HS footprint "AUDIO-SHIELD-G1B5"	
1.0	1. AUDIO GND-AGND 内部切割改15mil 2. CBC49/CBC50/CBC51/CBC52/CBC56/CBC69/CR105/CR110 从DGND改成AGND	
1.1	1. For PCH Rev.C2	
1.2	1. AUDIO CR75/CR92 short pad 2. DDU1 PIN6/7 short 3. Fix AUDIO_AMP POP Noise	

# BLOCK DIAGRAM



(E)

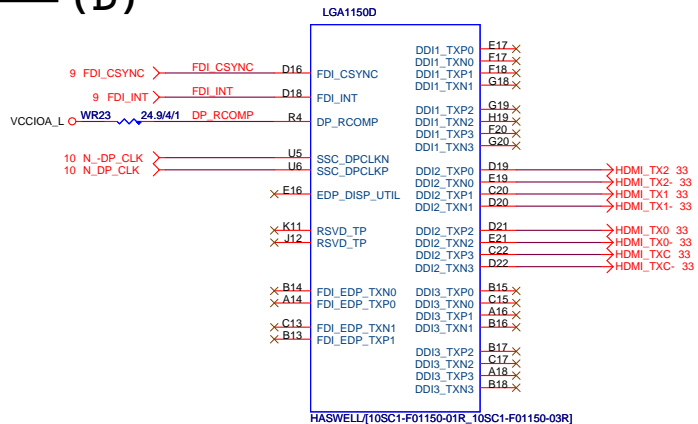


CFG	H	L	NOTE
0	R5VD	R5VD	R5VD
1	R5VD	R5VD	R5VD
2	ROHM	Reverse	LANE REVERSAL[0],x16
3	R5VD	R5VD	R5VD
4	Disable	Enable	eDP Enable
7	R5VD	R5VD	R5VD
8	R5VD	R5VD	R5VD
9	R5VD	R5VD	R5VD
10	R5VD	R5VD	R5VD
11	R5VD	R5VD	R5VD
12	R5VD	R5VD	R5VD
13	R5VD	R5VD	R5VD
14	R5VD	R5VD	R5VD
15	R5VD	R5VD	R5VD
16	R5VD	R5VD	R5VD
17	R5VD	R5VD	R5VD

CFG6	CFG5	PCIE CONFIG
1	1	1x16 , Default
1	0	2x8
0	1	RSVD
0	0	x8.x4.x4

CFG 0-17 all internal PULL-UP

(D)



FDI:15/4/4/4/15(breakout min 4/4/4//8)  
Impedance=85 +- 15%

DP/HDMI 15/4/4/4//15      FDI 12/4/4/4/12

Impedance=85 +- 15%

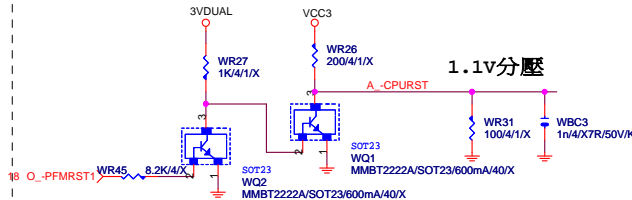
(c)



-----  
CPU PEG 20/5/4/5/20 Impedance=80 +- 15%

DMI 12/4/4/4//12 Impedance=85 +- 15%

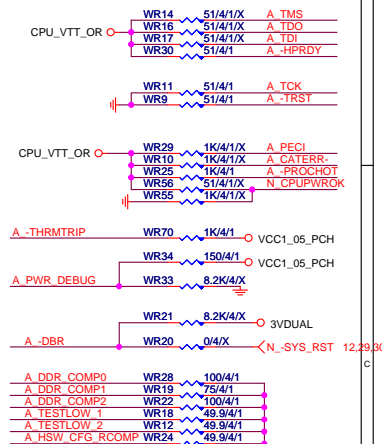
**-CPURST**



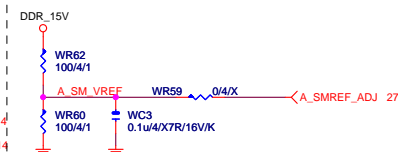
## CPU SVID



## CPU PU/PD



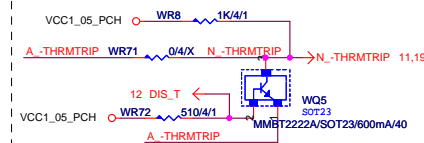
SM REF
--------



```

| THRMTRIP DISABLE FOR Z87 OVERCLOCK

```



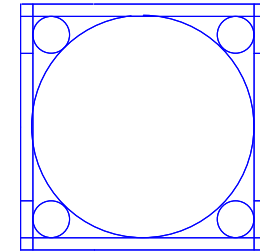
## LGA1150A

HASWELL/[10SC1-F01150-01R\_10SC1-F01150-03R]



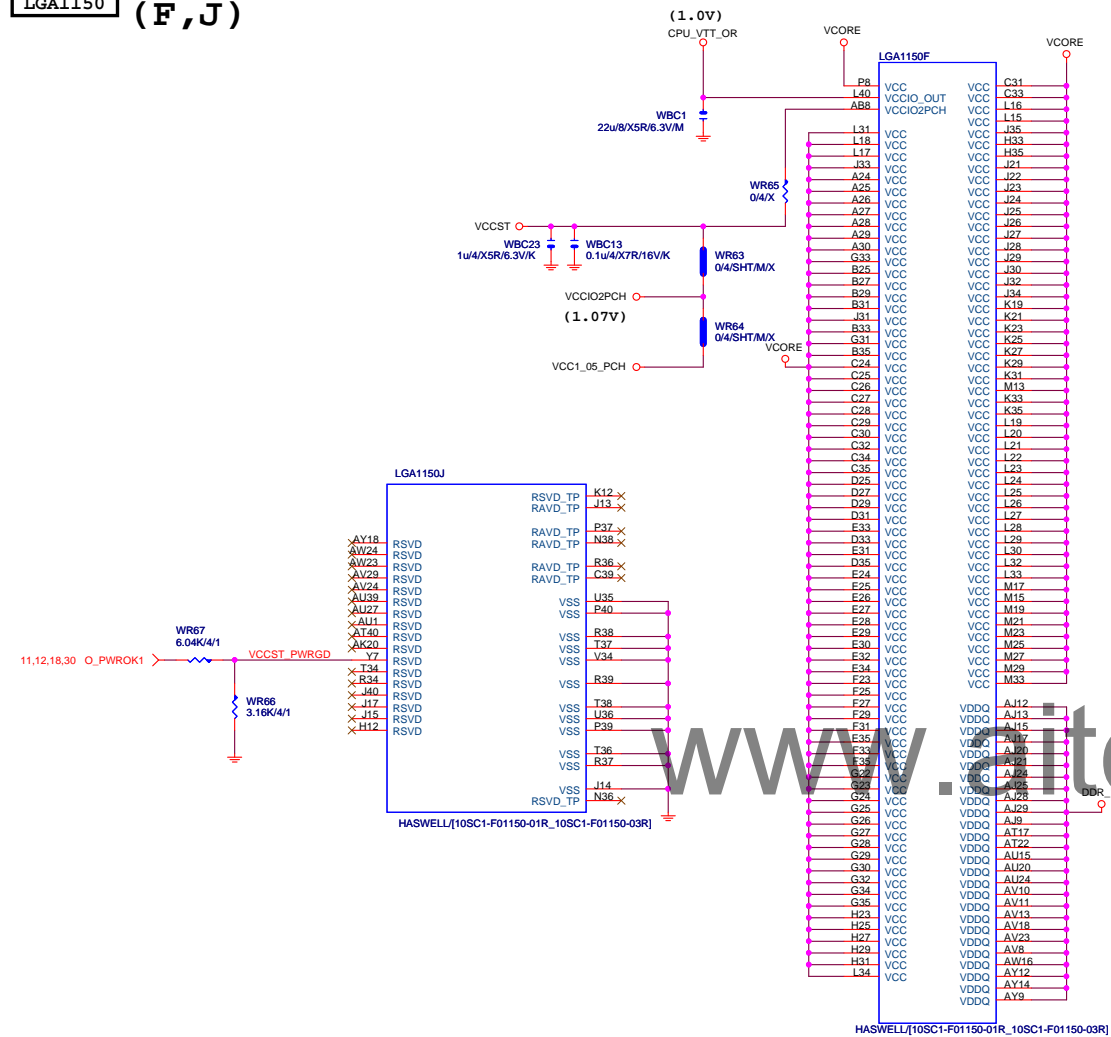
HASWELL/[10SC1-F01150-01R\_10SC1-F01150-03R]

LGA1150  
ILM\_BP/1156/BKNI/[12KRC-0F0001-61R\_12KRC-0F0001-62R]



7 MODT\_A[0..3] ↔ MODT\_A[0..3]  
 8 MODT\_B[0..3] ↔ MODT\_B[0..3]  
 7 MDA[0..63] ↔ MDA[0..63]  
 8 MDB[0..63] ↔ MDB[0..63]  
 7 DQSA[0..7] ↔ DQSA[0..7]  
 7 -DQSA[0..7] ↔ -DQSA[0..7]  
 7 MAAA[0..15] ↔ MAAA[0..15]  
 8 MAAB[0..15] ↔ MAAB[0..15]  
 8 DQSB[0..7] ↔ DQSB[0..7]  
 8 -DQSB[0..7] ↔ -DQSB[0..7]

**LGA1150 (F,J)**

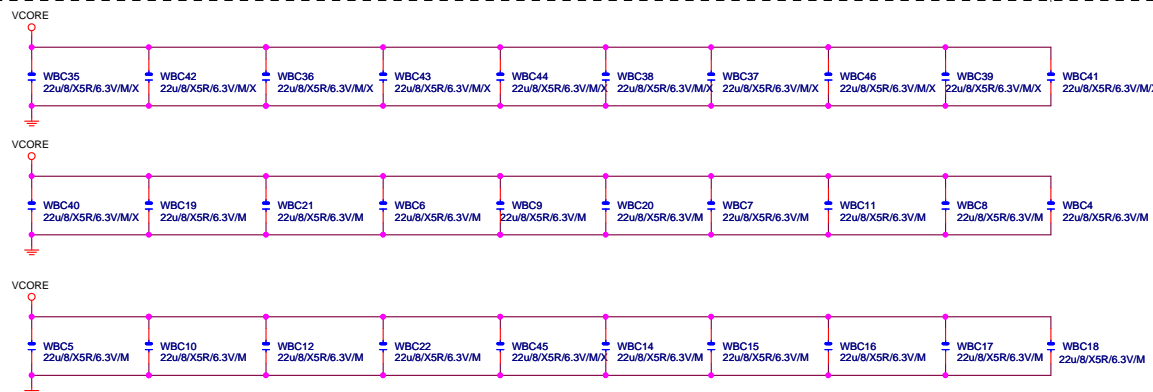


**LGA1150 (G,H,I)**



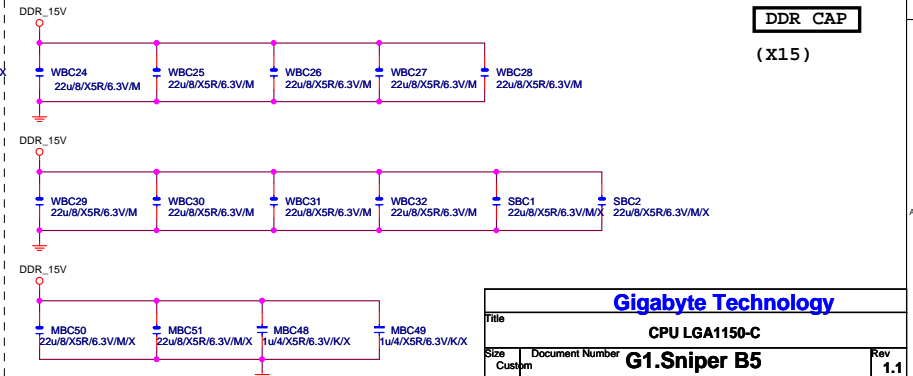
## VCore CAP

(X30)

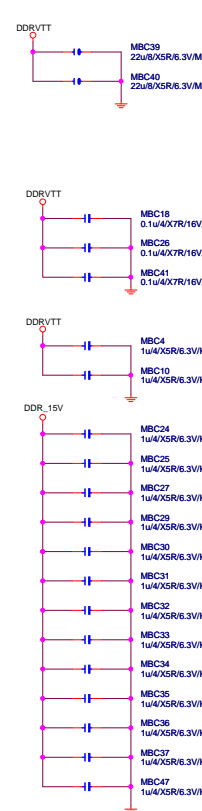
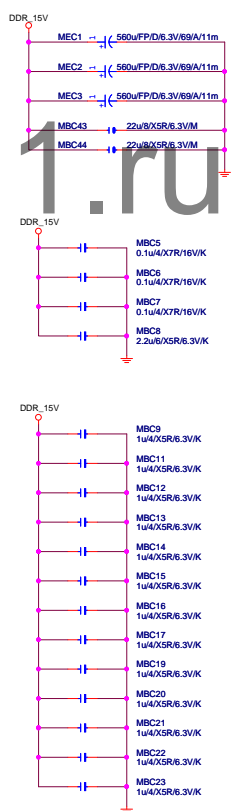
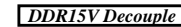
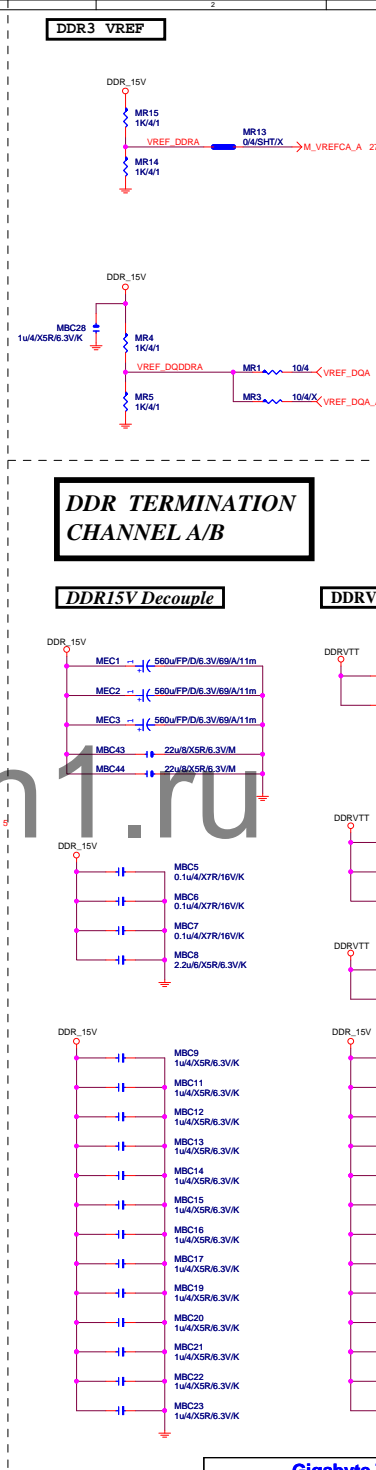
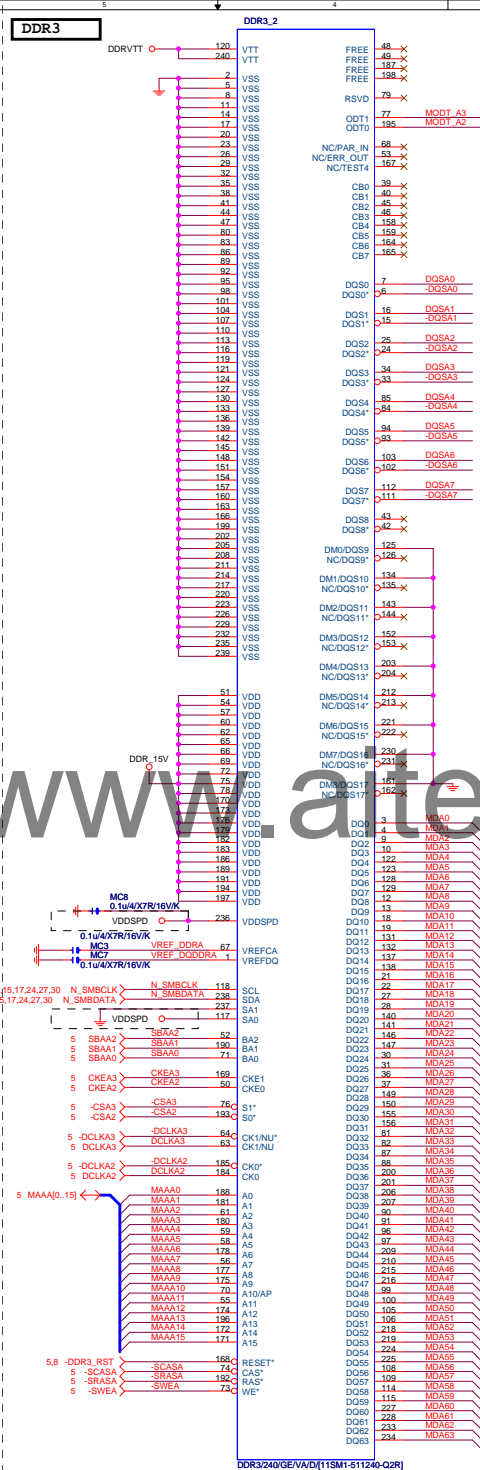


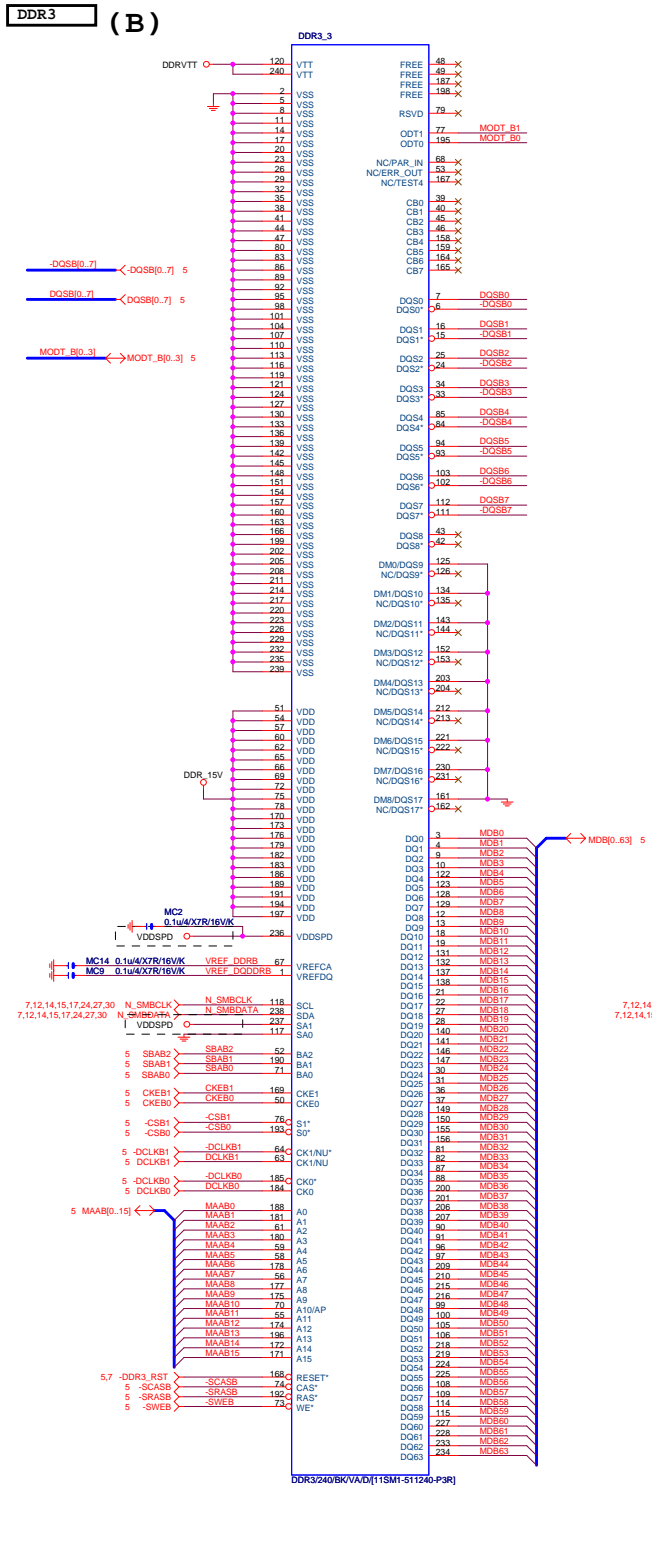
DDR CAP

(X15)





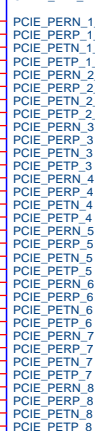
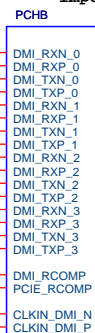






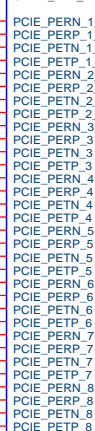
(B)

USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)  
Impedance=85 +/- 15%



PCIEX4 port4

放靠近 Device & PCI-E Slot



DH82B85/S/[10HB1-030B85-20R]

PCH PCIE ,DMI 15/4/4/4//15 Impedance=85 +- 15%

usb2.0 12/5/7/5/12

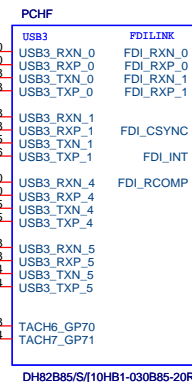
Impedance=85 +- 15%

(J)



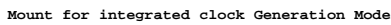
DH82B85/S/[10HB1-030B85-20R]

**(F)**

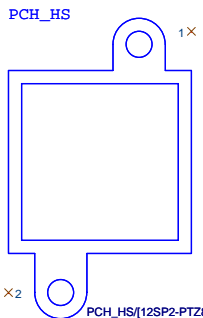


FDI:12/4/4/4/12  
Impedance=85 +- 17.5%

USB3.0:20/5/7/5/20 (breakout min  
8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS



PCH H/S



## USB TABLE

```
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)
```

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

## Gigabyte Technology

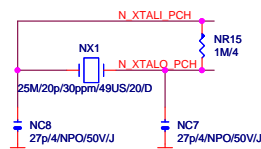
Title			
PCH FDI,DMI,USB ,PCIE			
Size	Document Number	Rev	
Custom		1.1	
G1.Sniper B5			
Date:	Thursday, June 27, 2013	Sheet	9 of 34

Timing diagram for PCHC signals. The diagram shows a blue box containing signals: DDPB\_HPD, DDPB\_HPD, DDPD\_HPD, VGA\_RED, VGA\_GREEN, VGA\_BLUE, VGA\_IRTN, VGA\_DDC\_DATA, VGA\_DDC\_CLK, VGA\_DDC\_REF, DDPB\_CTRLCLK, DDPB\_CTRLDATA, DDPB\_CTRLDATA, DDPD\_CTRLCLK, DDPD\_CTRLDATA, and DDPD\_CTRLDATA. External signals include AH3, AH4, AC2, AC3, AG4, AL3, AL2, AF5, AN3, AM2, AM1, AJ5, AN4, and AN2. Timing constraints are shown: VGA 4/20; +-200MILS; GND REF, DDC DIFF 4/5; +-1000, and IREF 4/12; +-500MILS; GND. A note at the bottom reads DH82B85/S(10HB1-030B85-20R).

VGA_DISABLE
R,G,B NC OR GND
IRTN / IREF GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA NC
POWER_VCCADAC(AF2) GND, VCCADACBG(AE1) GND

PCH FDI_RXP[0:1] NC
PCH FDI_RXN[0:1] NC
CPU FDI_TXP[0:1] NC
CPU FDI_TXN[0:1] NC
FDI_RCOMP NC
<b>FDI_IREF (N11)</b>

Flex1,2,3,4 :  
14/24/33/48MHZ



N_XTALO_PCH	N7	XTAL25_OUT	CLKOUT_
N_XTALI_PCH	N6	XTAL25_IN	CLKOUT_
			CLKOUT_
			CLKOUT_

DH82B85/S[10HB1-030B85-20R]

Differential Clock:18/4/6/4/18  
Impedance=90 +- 15%

NR42 8.2K/4  
NR41 8.2K/4

Mount for integrated clock Generation Mode

## VGA DDC

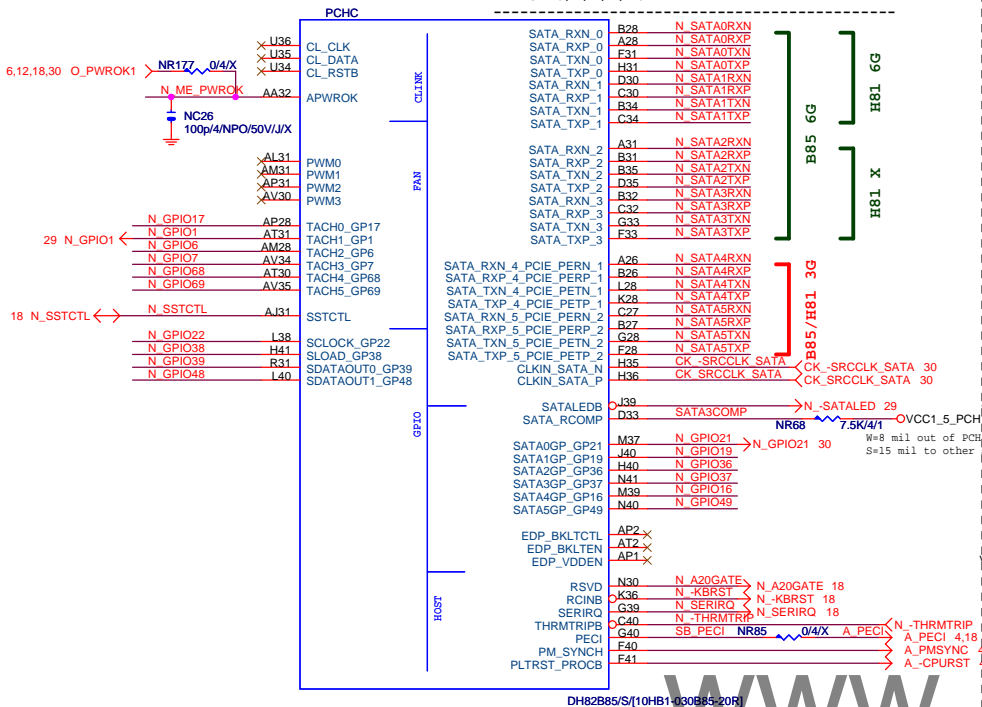
**PCH (C)**

SATA3 : 20/4/4/4/20 (breakout min 8/4/4/4/8)

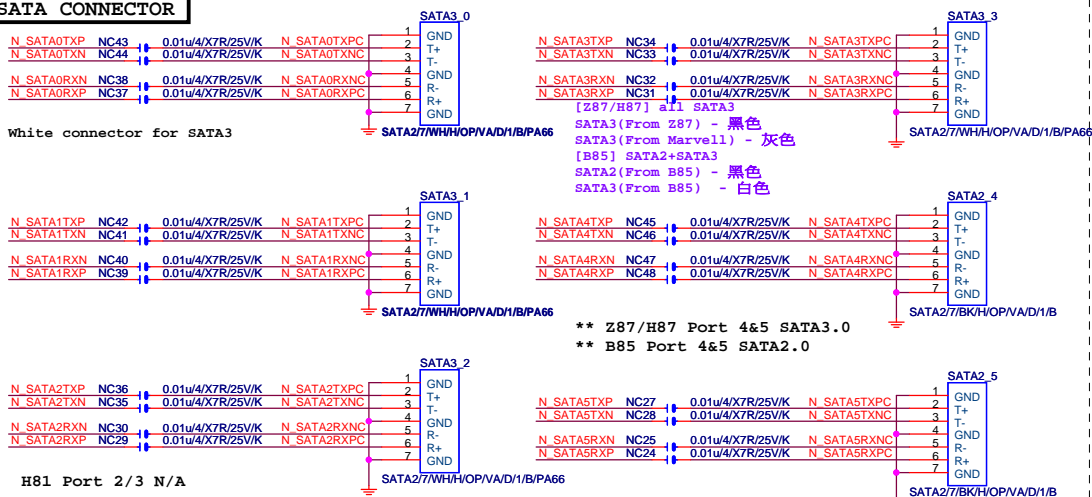
Impedance=85 +- 17.5%

SATA2 15/4/4/4/15

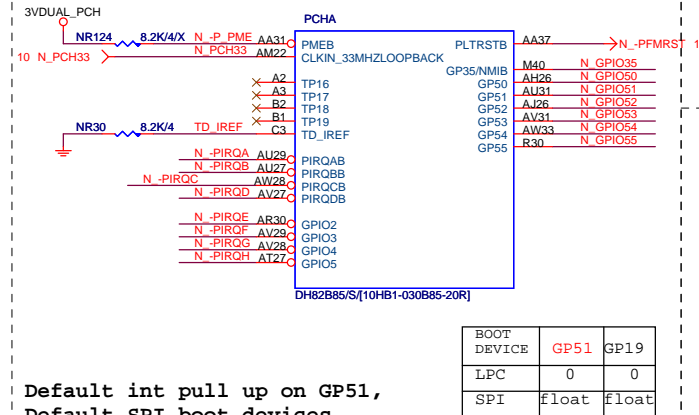
SATA3 20/4/4/4/20



## SATA CONNECTOR

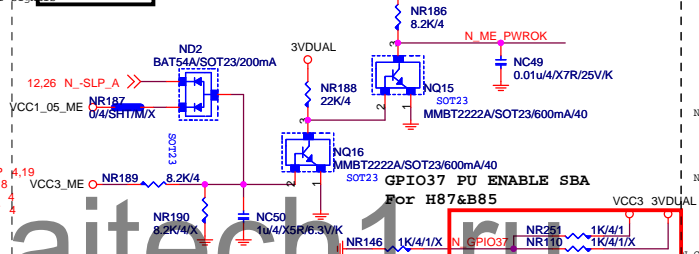


**PCH (A)**



```
Default int pull up on GP51,  
Default SPI boot devices
```

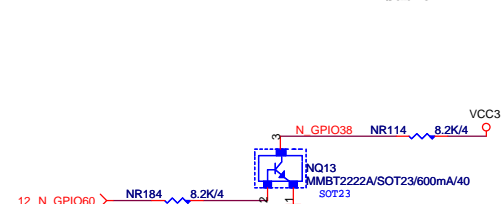
ME PWROK



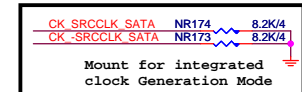
GPIO38 Ctrl

MFG Mode

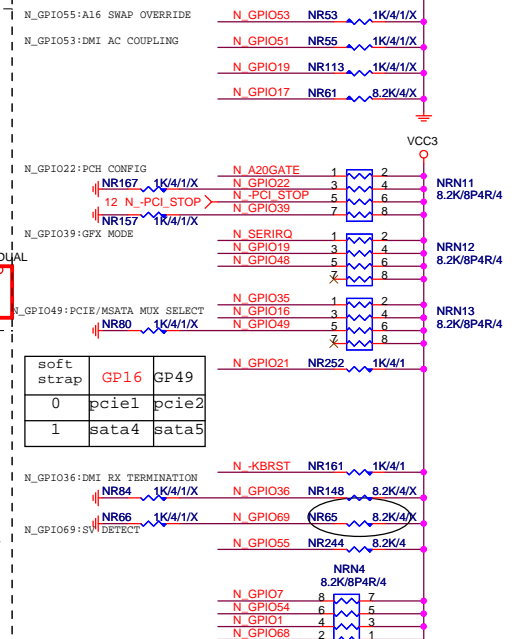
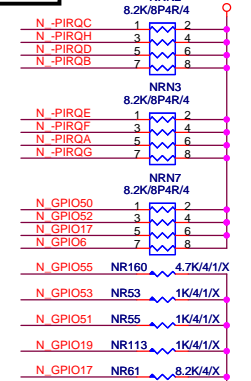
```
N_GPIO38 : Lo --> Enable
           Hi --> Disable
```



PCH	CLK	PD
-----	-----	----



PCH	PU/PD
-----	-------

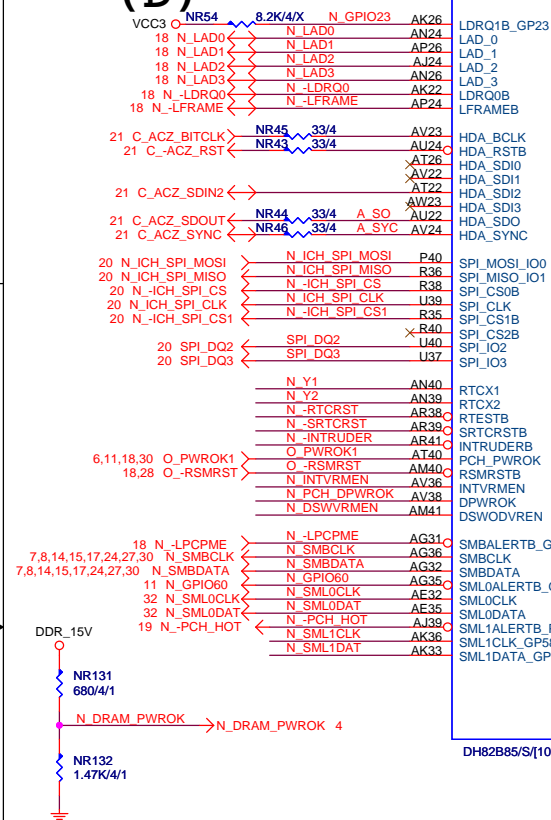


## Gigabyte Technology

Title			
PCH HOST , SATA, PCI			
Size	Document Number	Rev	
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Date:	Thursday, June 27, 2013	Sheet	11 of 34

## PCH

(D)



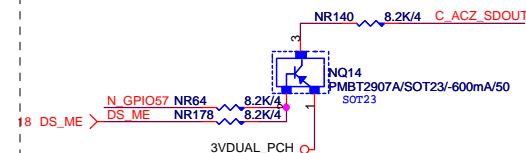
## PCHD

DH82B85/S[10HB1-030B85-20R]

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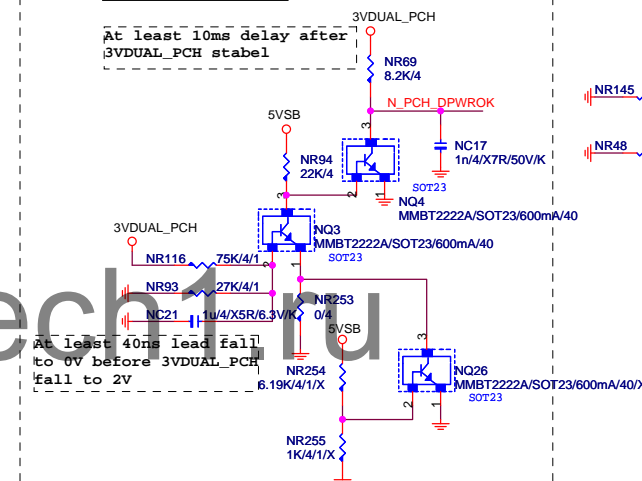
## ACZ\_SDOUT

C\_ACZ\_SDOUT : HI --> ME Enable  
Lo --> ME Disable  
HI:disable ME and override SPI Flash Access Permissions



## PCH\_DPWROK

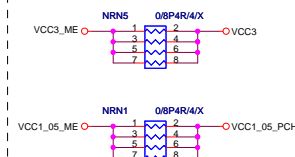
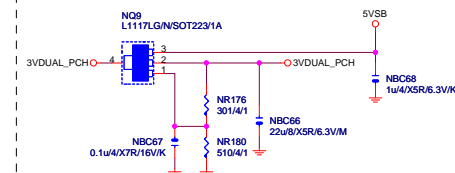
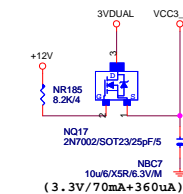
At least 10ms delay after 3VDUAL\_PCH stabel



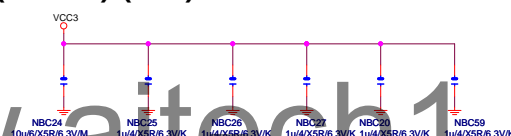
**PCH (I)**



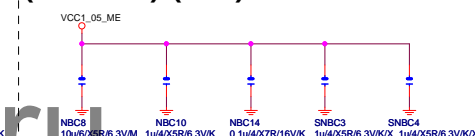
SHT PWR



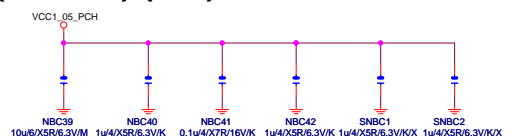
( 3.3V ) ( X6 )



(1.05V) (x5)



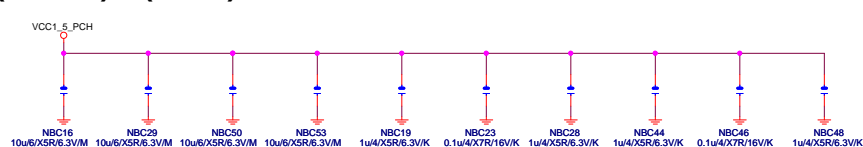
(1.05V) (x6)



(1.05V)(x2) (3.3V) (x2)

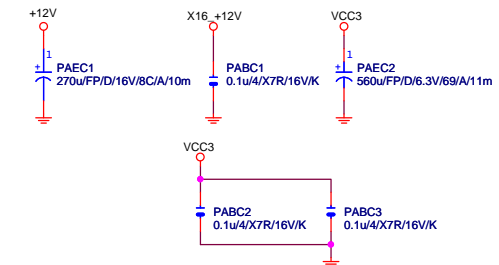


(1.5V) (x10)



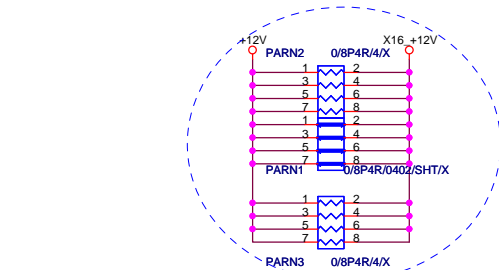


# PCIEX16 CAP



# PCIEX16 PROTECT SHT

+12 protect short-wire test



# PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

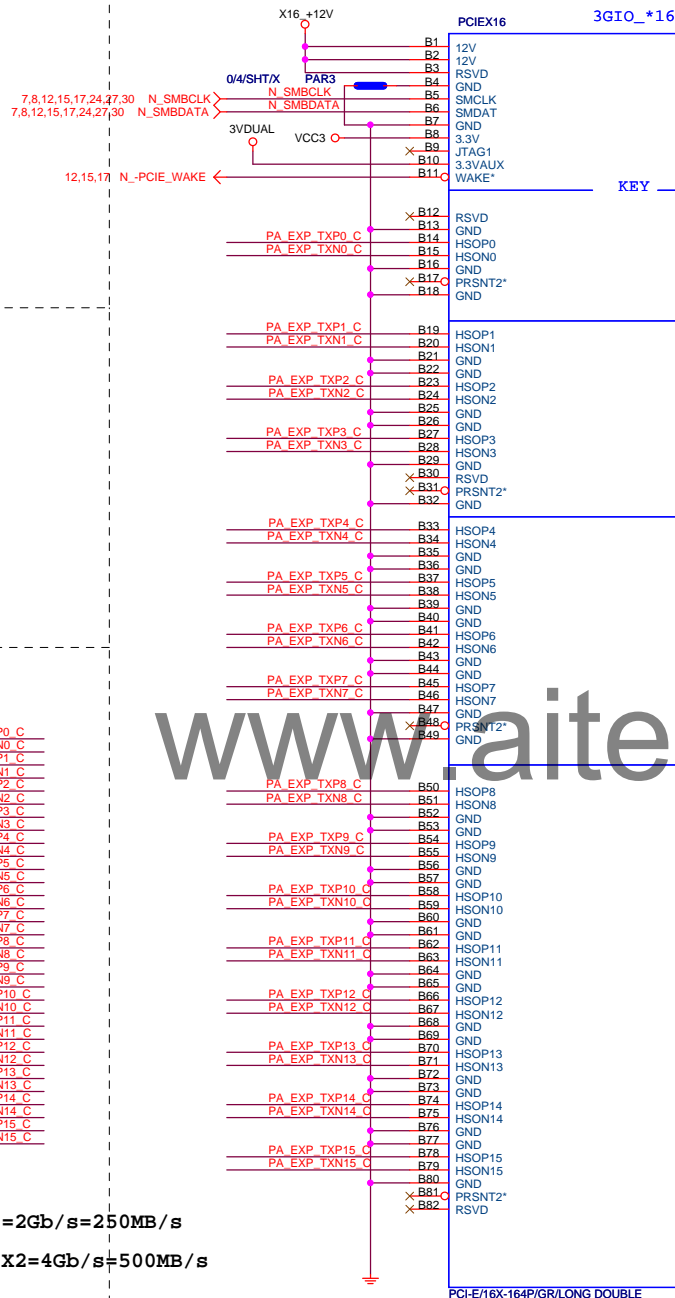
PCE-E X1(雙向) BANDWITH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

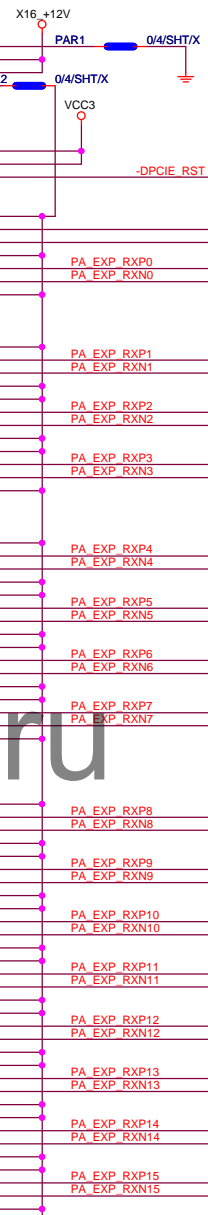
# PCIEX16 SLOT



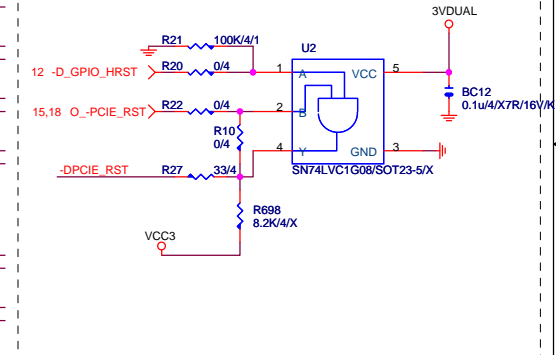
PCIESLOT-164DN-Q

3GIO\_16

PCI-E/16X-164P/GR/LONG DOUBLE



The auxiliary reset circuit is only required for PCIe Gen3 margining and functional link training



PCIEX16:16/5/5/5/16

PA EXP RXP10.15I >>> PA\_EXP\_RXP[0..15] 4  
PA EXP RXN10.15I >>> PA\_EXP\_RXN[0..15] 4  
PA EXP TXP10.15I >>> PA\_EXP\_TXP[0..15] 4  
PA EXP TXN10.15I >>> PA\_EXP\_TXN[0..15] 4

Gigabyte Technology

Title			
PCI EXPRESS * 16			
Size	Document Number	Rev	
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## SIO IT8728F

SYS\_FAN3

12 DS\_ME  
31 FANPWM4  
19 RTS1-  
19 DSR1-  
19 TXD1  
19 RXD1  
19 DTR1  
19 DCD1-  
19 RI1

CPU\_FAN

SYS\_FAN1

SYS\_FAN2

IT8728F (GB)

【技術通報R&D技術通報151】  
有使用PRINT PORTの MODEL  
需使用新料號:10HP2-118728-72R

IT8728F/EX (GB)/QFP128[10HP2-118728-72R]

R&D技術通報151 有使用PRINT PORTの  
MODEL・需使用新料號:10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD  
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

For IT8728  
A\_PECI 4.11  
N\_SSTCTL 11

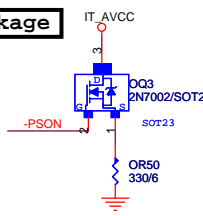
## IT8728F NOTE

	IT8728
PIN121	VCORE_EN#/PCH_C0
PIN120	VLDT_EN#/PCH_D0
PIN19	ATXPG
PIN31	PCH_C1
PIN53	SST/AMDTSL_D/MTRB#/PCH_D1
PIN55	PECI/AMDTSL_C/DRV#
PIN66	SYS_3VSB
PIN70	GP47
PIN95	VIN2(VCC5)
PIN96	VIN1(VCC12)
PIN97	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0/VCORE(1.1V)/NC

## DUAL BIOS OPT STRAP



## Power leakage

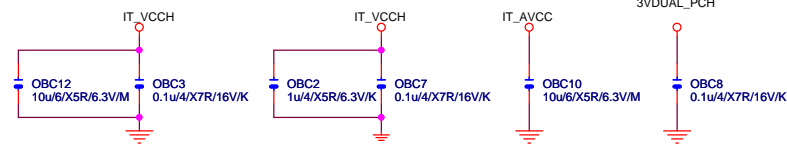


## SIO\_18V

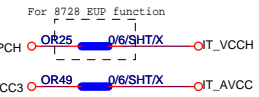
internal power pin, max 22nF cap



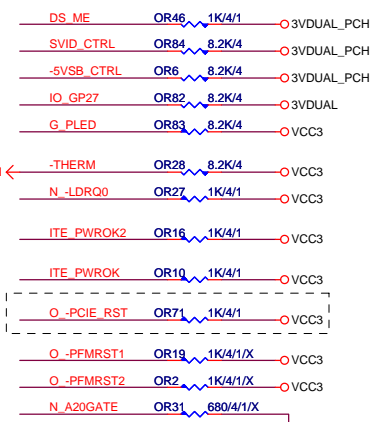
## SIO CAP



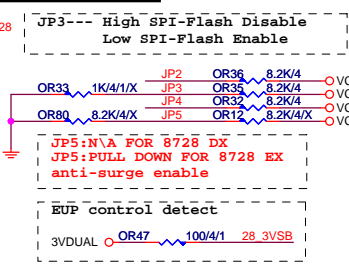
## PWR SHT



## SIO PU

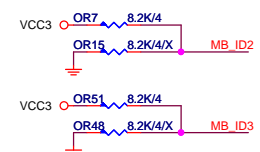


## SIO STRAP



JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	0 1	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	1 0	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

## MB ID

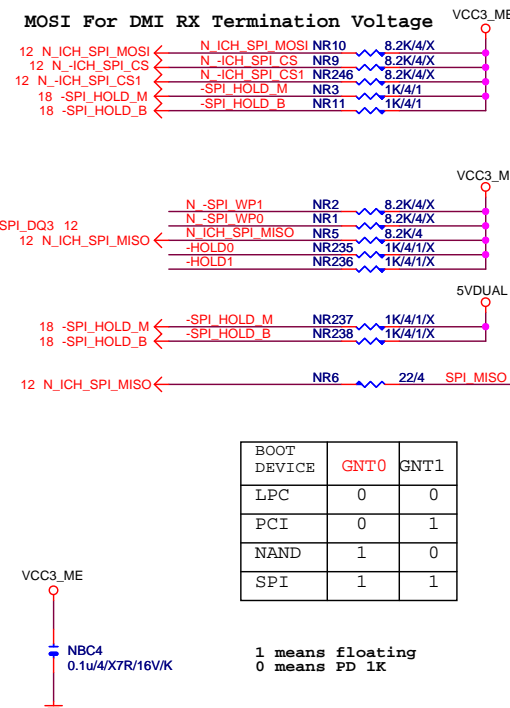
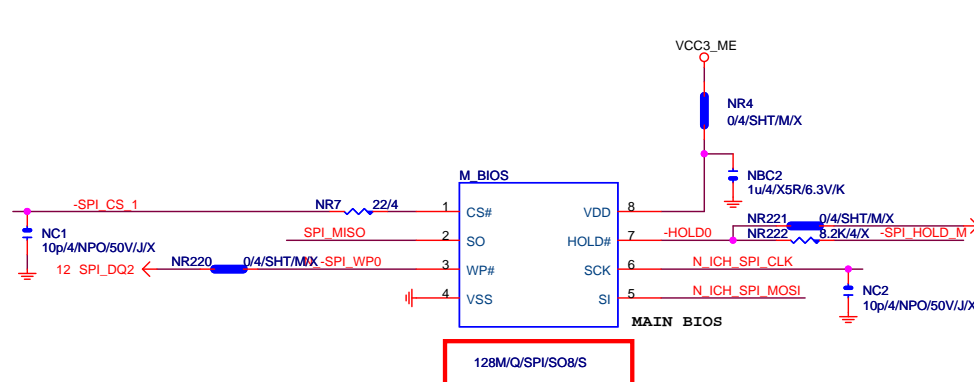
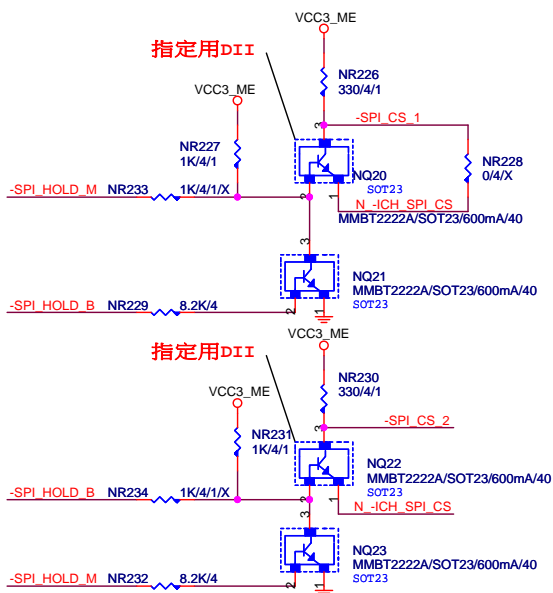


Gigabyte Technology

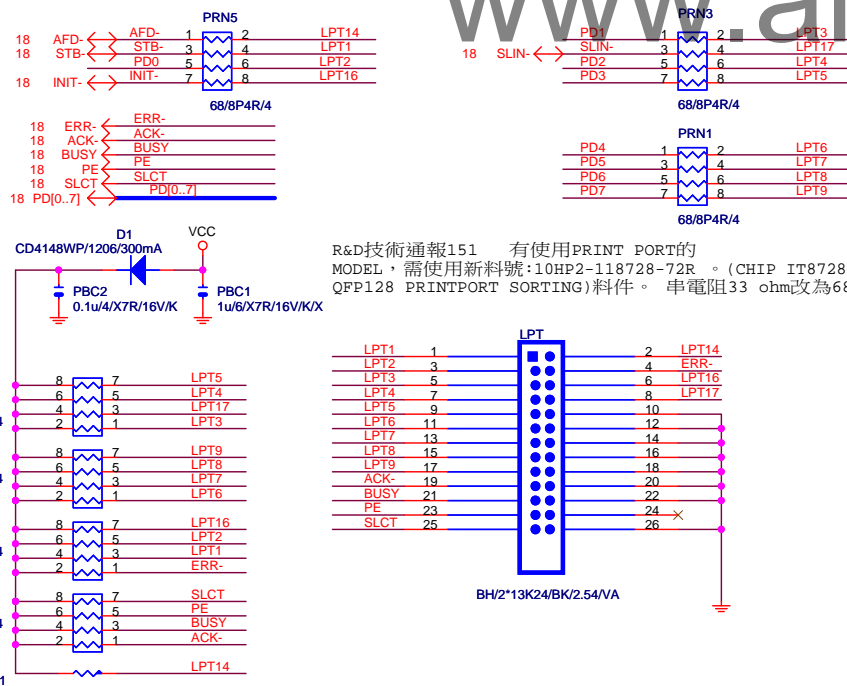
Title			ITE 8728 LPC IO	
Size B	Document Number		G1.Sniper B5	
Date:	Monday, July 01, 2013	Sheet	18	of 34
Rev		1.1		



## DUAL BIOS



## LPT PORT



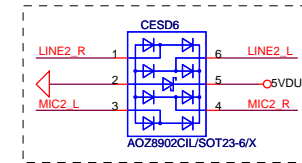
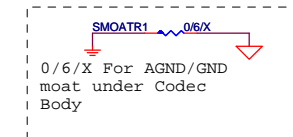
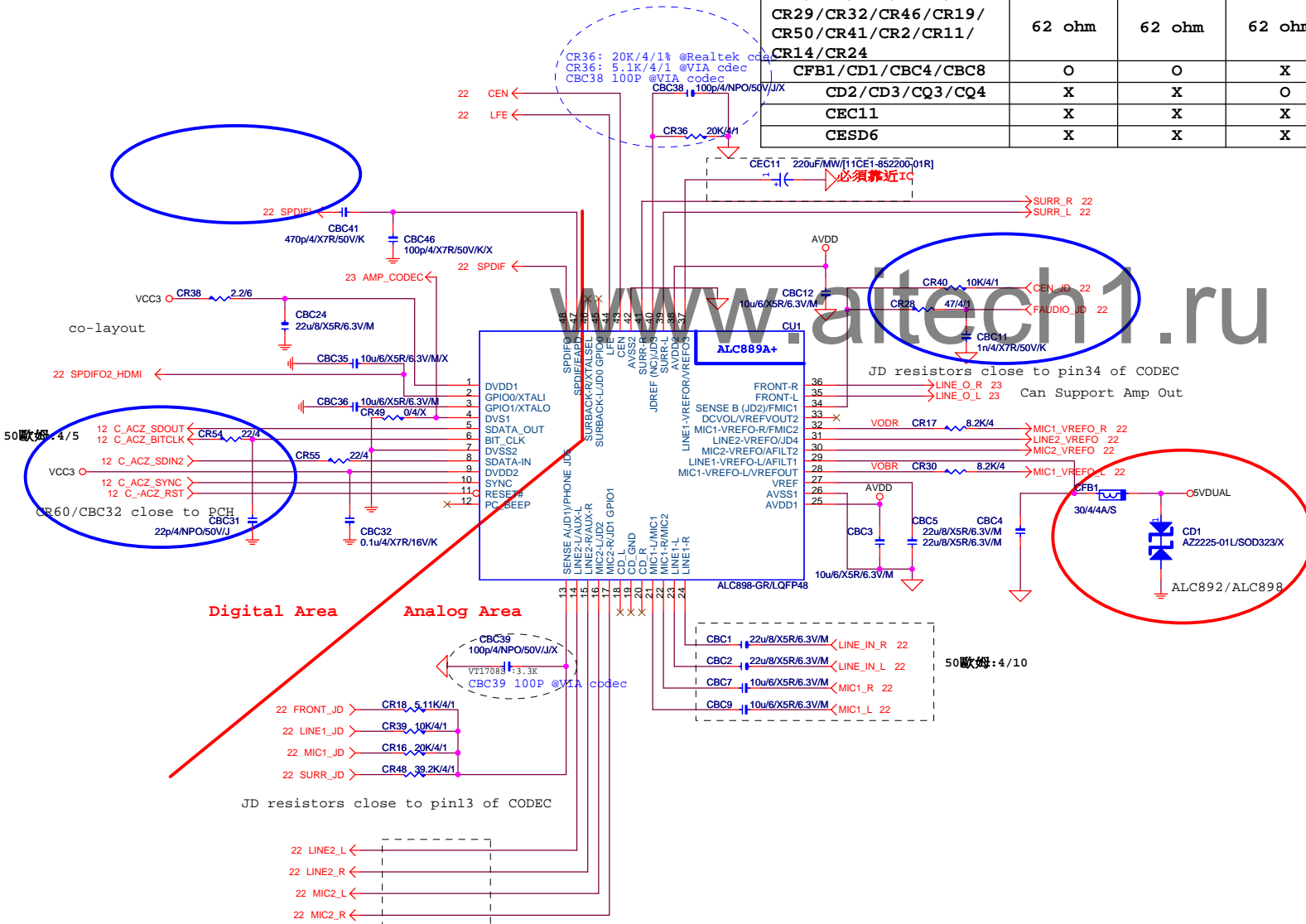
R&D技術通報151 有使用PRINT PORT的  
MODEL，需使用新料號：10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD  
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

```
1 means floating
0 means PD 1K
```

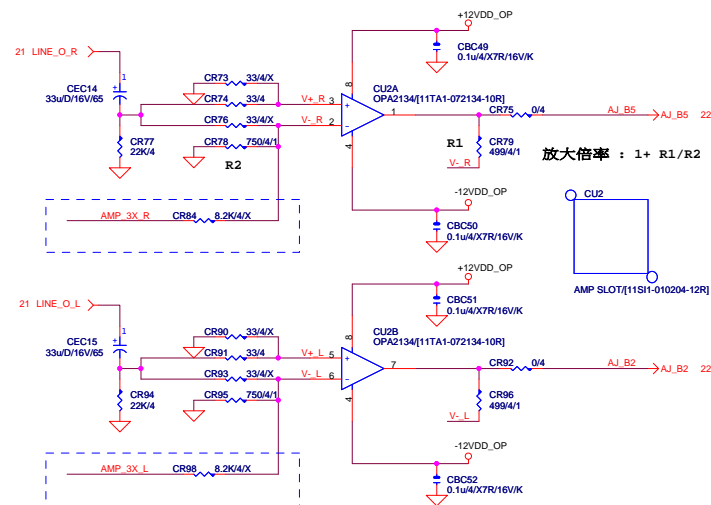


	ALC662	ALC887-VD2	ALC889	VT1708S-CD	VT1708S-CE	VT2021	ALC898/ALC892
CR49	X	X	O	O	X	O	X
CBC36	O	O	X	X	O	X	O
CR28/CBC11	47ohm+1nF	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P	47ohm+1nF	47ohm+1nF
CR52	X	O	O	O	O	O	O
CR57	O	X	X	X	X	X	X
CBC1/CBC2	10uF/X5R	10uF/X5R	22uF/X5R	10uF/X5R	10uF/X5R	10uF/X5R	22uF/X5R
CR36	20K/4/1	20K/4/1	20K/4/1	5.1K/4/1	20K/4/1	5.1K/4/1	20K/4/1
CR17/CR30/ CR25/CR15/CR12/CR3/	8.2K/4	8.2K/4	8.2K/4	3.3K/4/1	3.3K/4/1	3.3K/4/1	8.2K/4
CBC38/CBC39	X	X	X	100P/4	100P/4	X	X
CR10/CR8/CR20/CR45/ CR42/CR51/CR27/CR26	22K/4	22K/4	22K/4	10K/4/1	10K/4/1	10K/4/1	22K/4
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR2/CR11/ CR14/CR24	62 ohm	62 ohm	62 ohm	75 ohm	75 ohm	75 ohm	62 ohm
CFB1/CD1/CBC4/CBC8	O	O	X	X	O	X	O
CD2/CD3/CQ3/CQ4	X	X	O	O	X	O	X
CEC11	X	X	X	X	X	X	O
CESD6	X	X	X	O	O	O	X

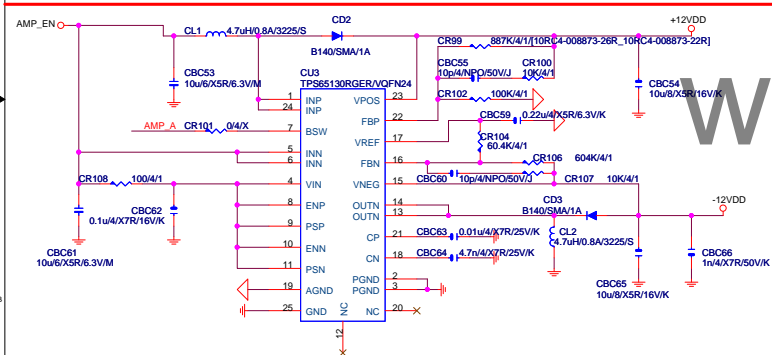
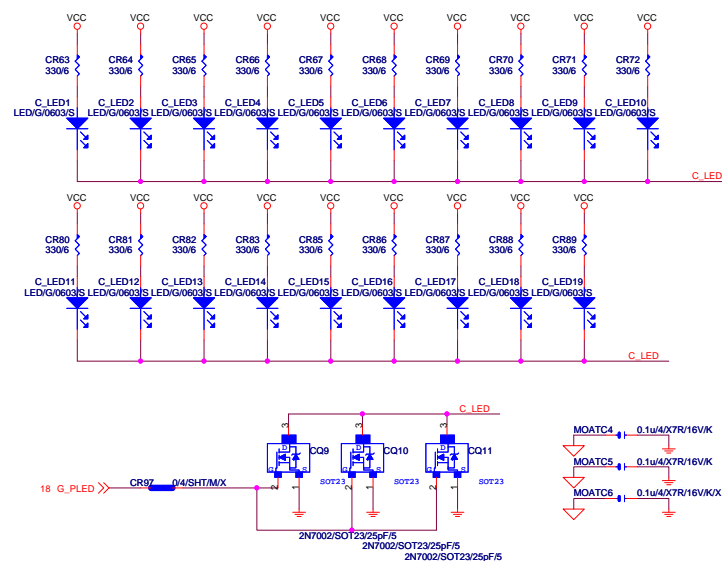




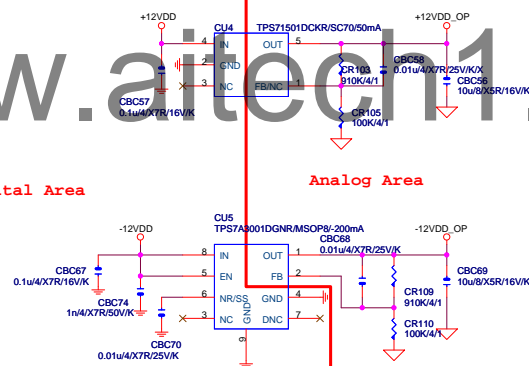
AMPLIFIED



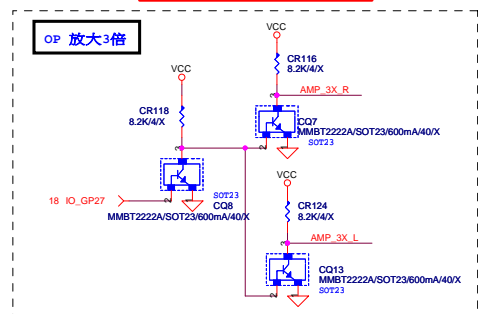
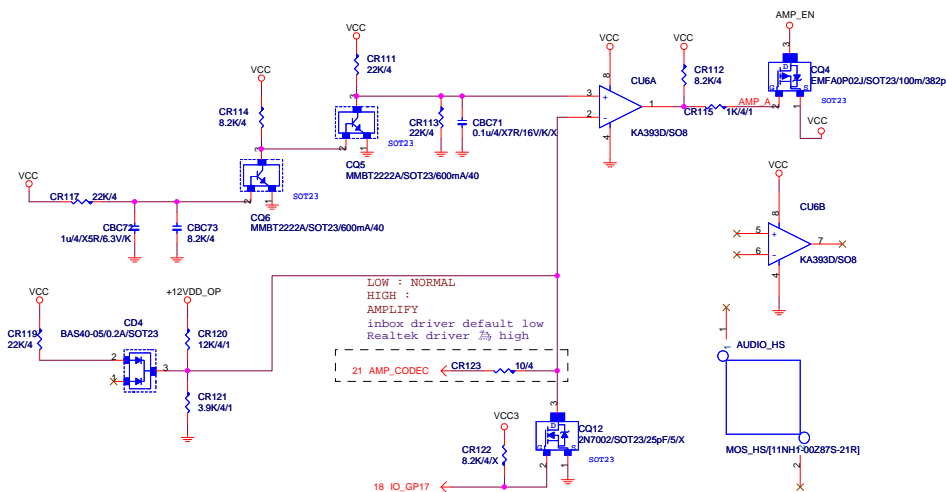
## Analog Area

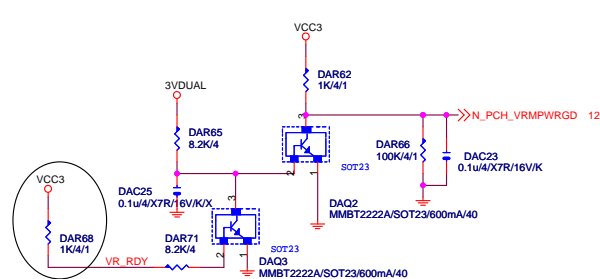
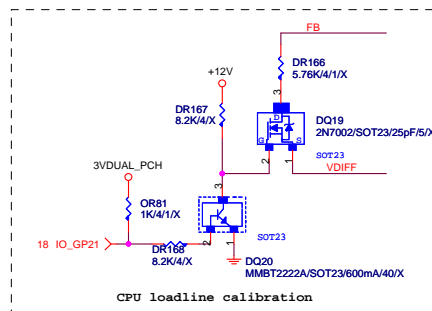
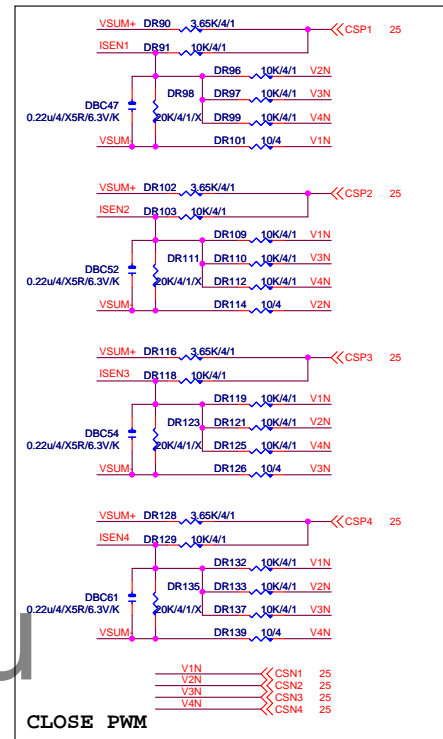
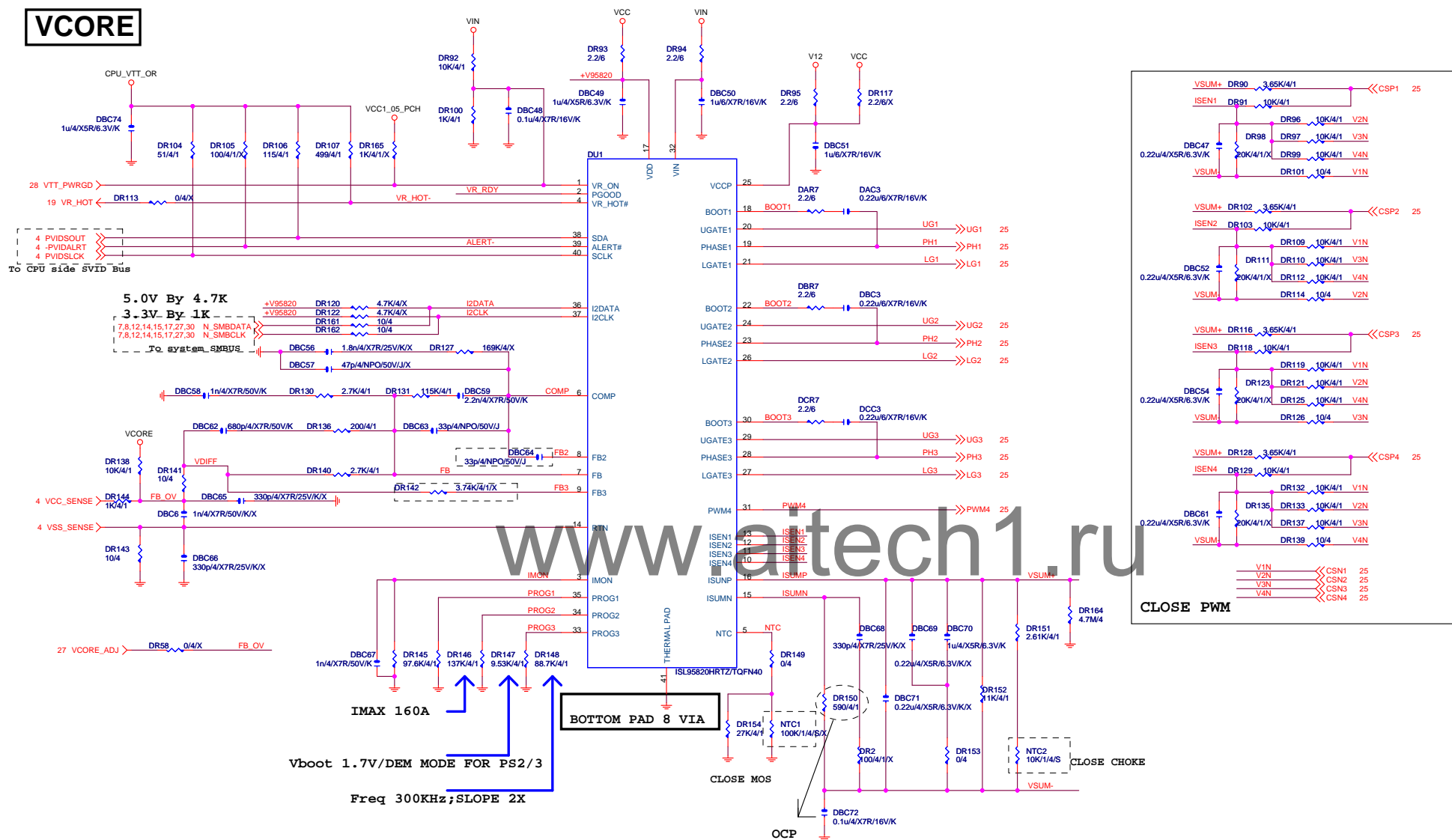


## Digital Area



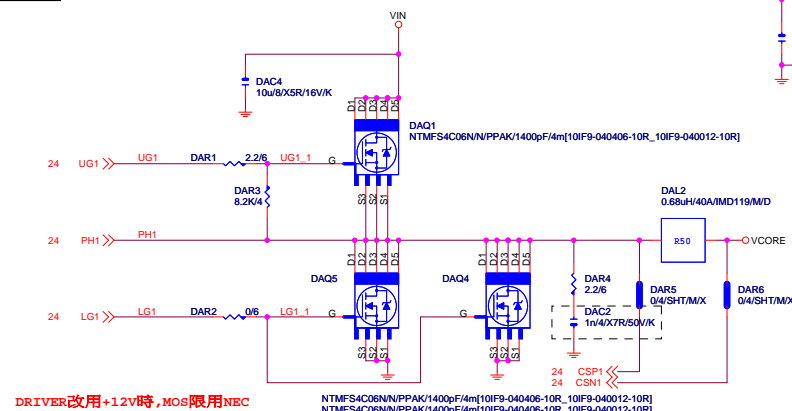
### Analog Area



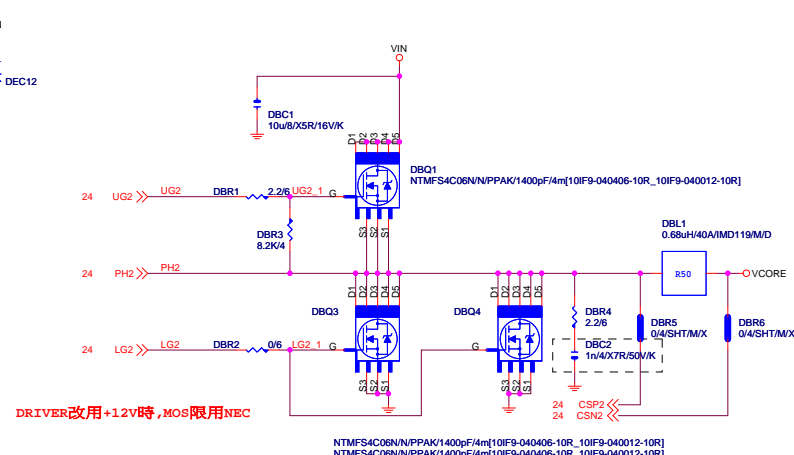
**VCORE**

# VCORE

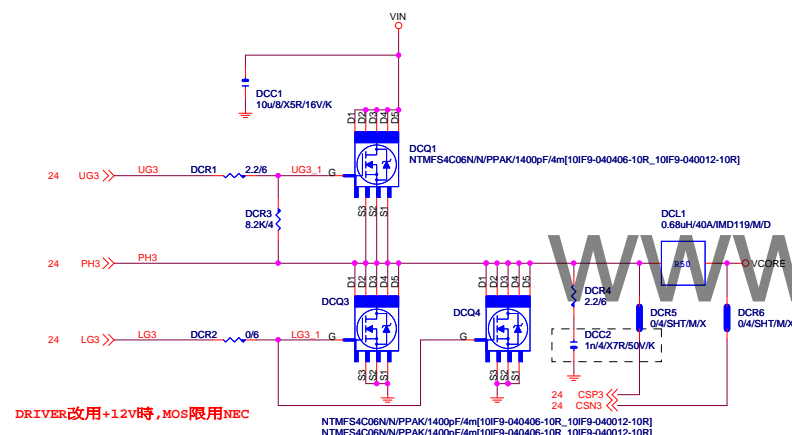
[1]



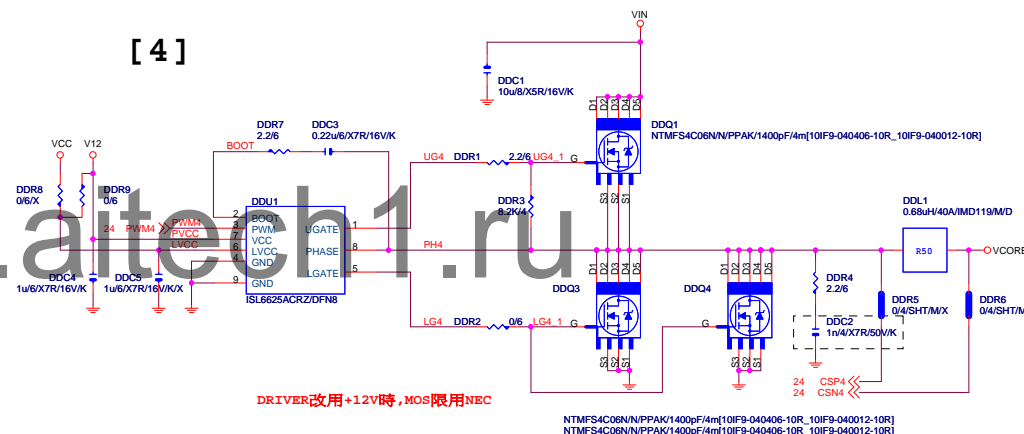
[2]



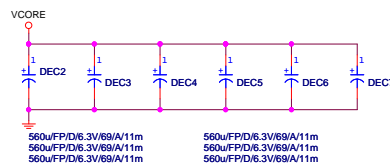
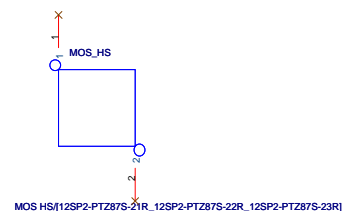
[3]



[4]



# MOSFET HEATSINK

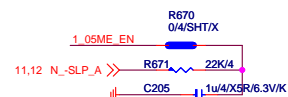
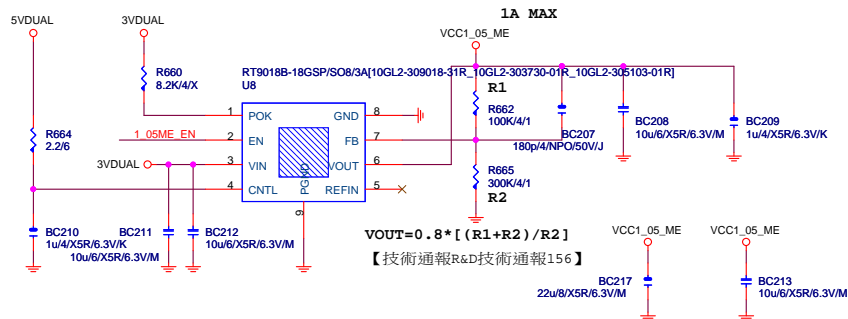


Gigabyte Technology			
Title		ISL95820_2	
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Date		Thursday, June 27, 2013	
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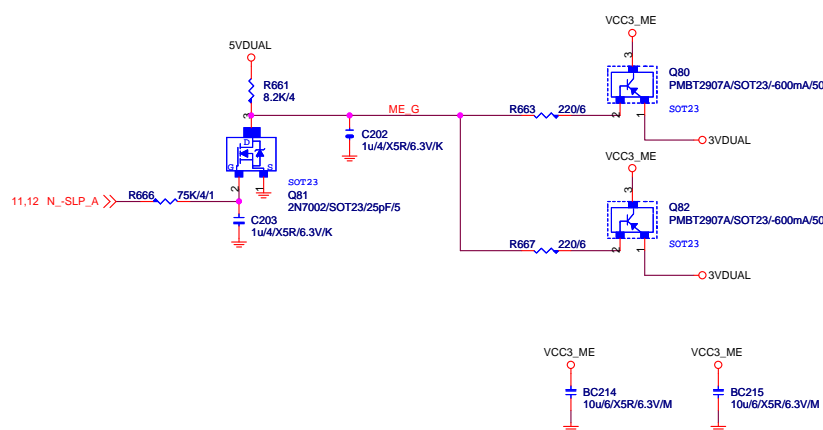
VCC1\_05\_ME

【技術通報R&amp;D技術通報156】

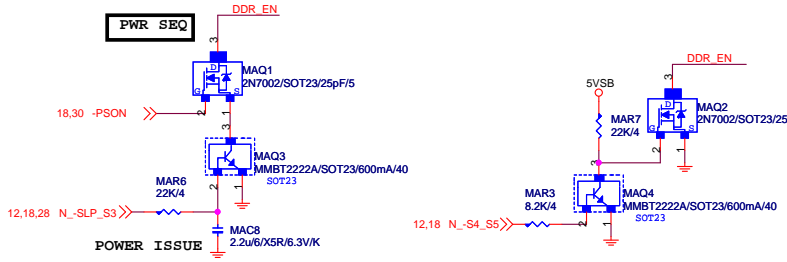
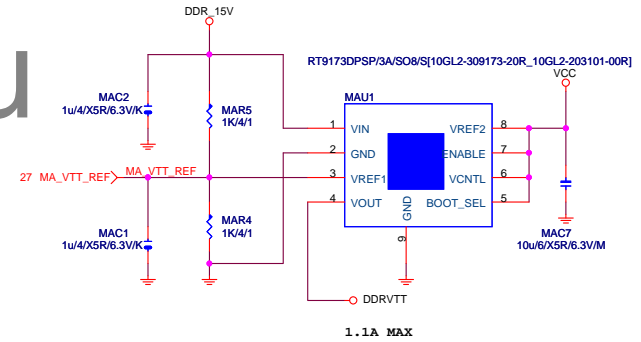
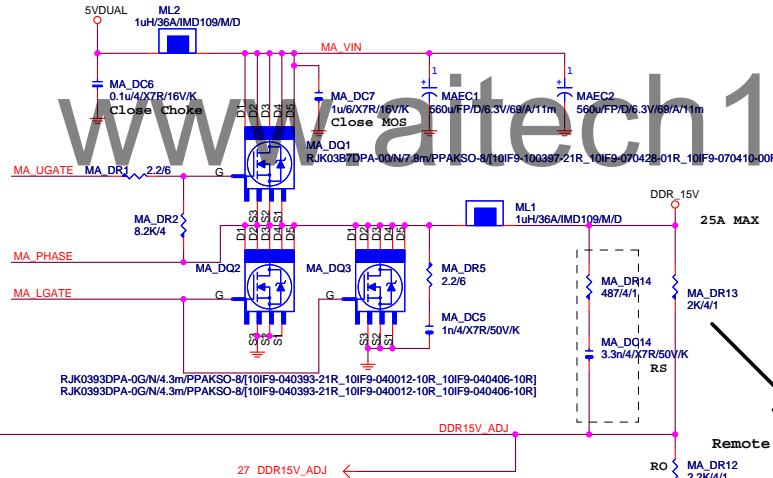
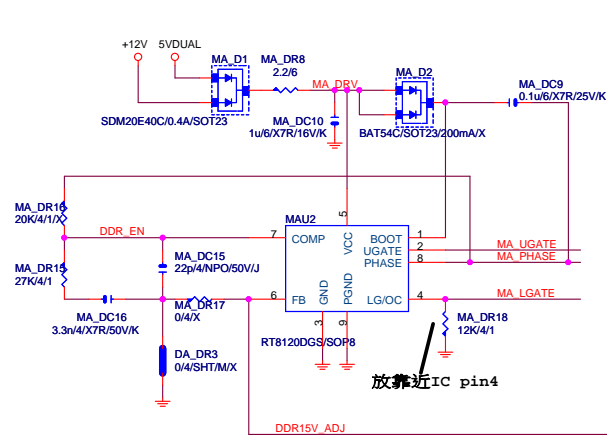
(RICHTER), (NUVOTON), (EMC) 做共用  
PIN7 分壓阻值須做修改為 100K 以上電阻值



## VCC3\_ME



**DDR\_15V**



VIN=5V,VOUT=1.5V,IOUT=25A,PHASE=1  
IRMS=11.45A

560uF/P/D/6.3V/68/8m RIPPLE CURRENT=4.7A  
Coefficient=1.7(85°C),1(105°C)  
VIN Ripple current=4.7X1.7=7.99A(85°C)  
-->故固態電容須2X7.99=15.98>11.45A

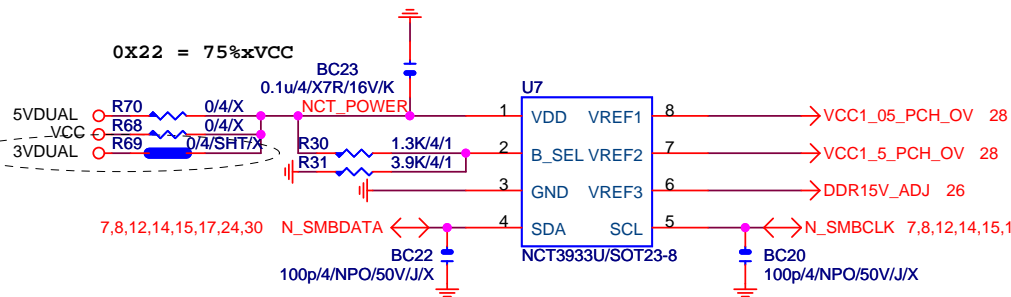
OCP:35.82A for Rds=6.7m for vishay@4.5V  
OCP:72.727A for Rds=3.3m for renesas@10V  
OCP:48A=Roset\*Iocset / Rds(on)  
=12K\*10uA / [5/5]

Remote sense 請從最重的負載端點拉回

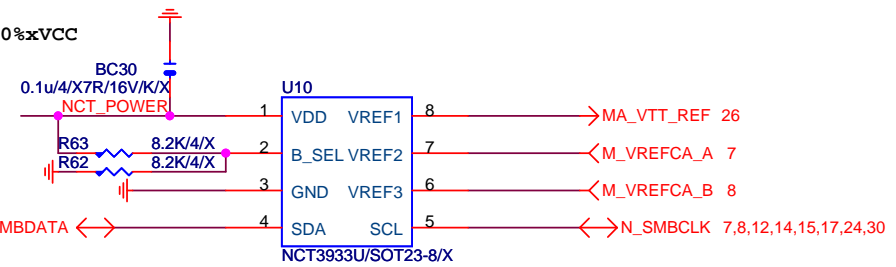
$$\begin{aligned} 0.8 \cdot (1 + R_S/R_O) &= V_{out} \\ 0.8 \cdot [1 + 2K/2.2K] &= \\ 1.527V \end{aligned}$$



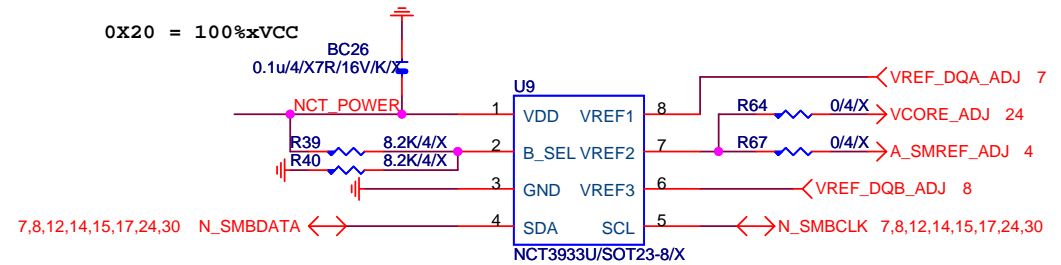
# OVER VOLTAGE



0X2A = 0%xVCC



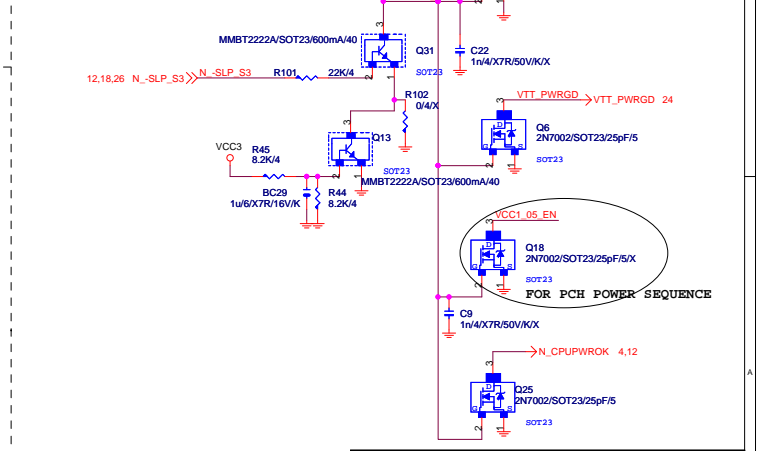
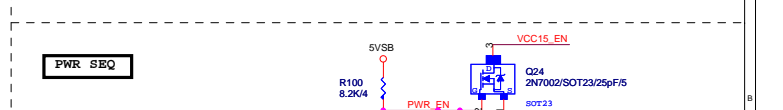
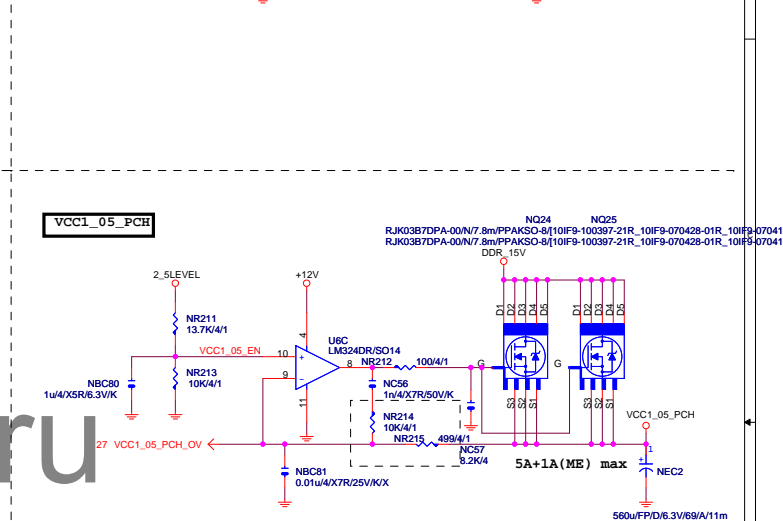
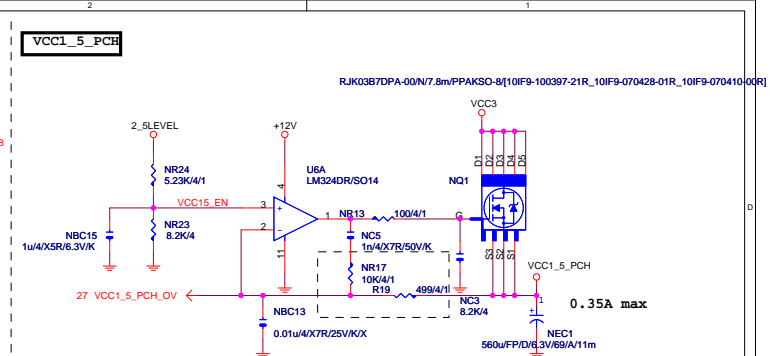
0X20 = 100%xVCC



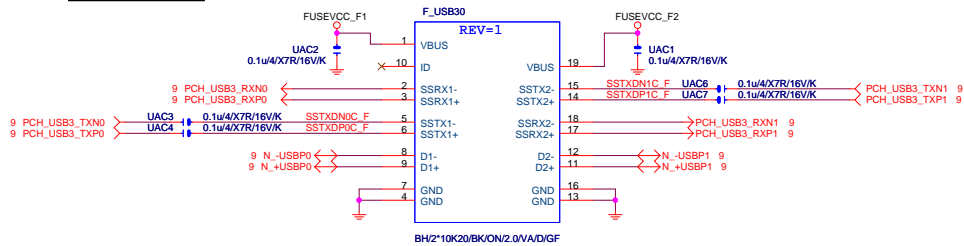
NCT3933	0X2A	0X20	0X22
VREF1	DDRVT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

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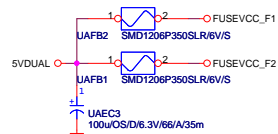
Title			
CPU CORE VR-2			
Size	Document Number	G1.Sniper B5	
Custom		Rev 1.1	
Date:	Thursday, June 27, 2013	Sheet	27 of 34



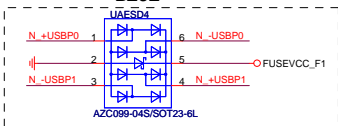
## Front USB3.0



F\_USB30 PWR

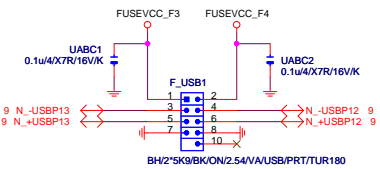


**BLUE**

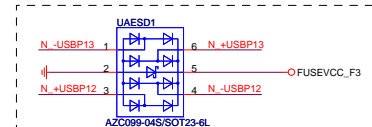


Close to connector

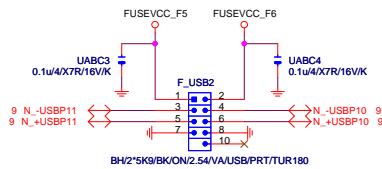
FRONT USB1



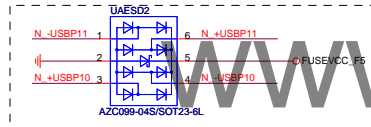
Close to connector



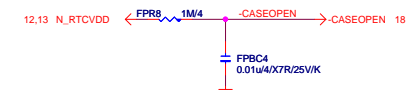
FRONT USB2



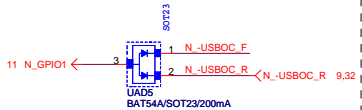
Close to connector



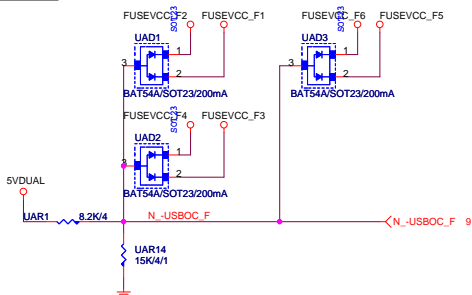
## CASE OPEN



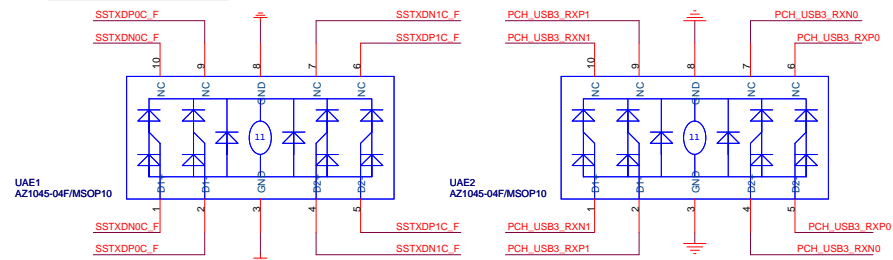
F_USB POWER PROTECT
---------------------



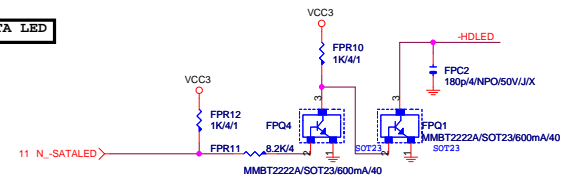
-USBOC\_F



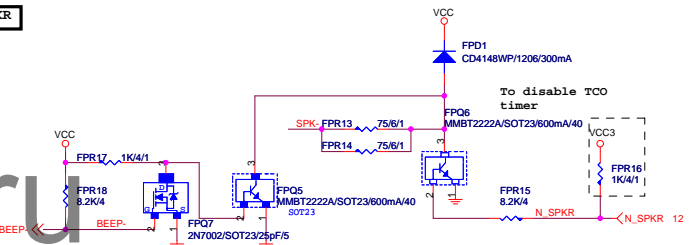
F_USB30 ESD PROTECT
---------------------



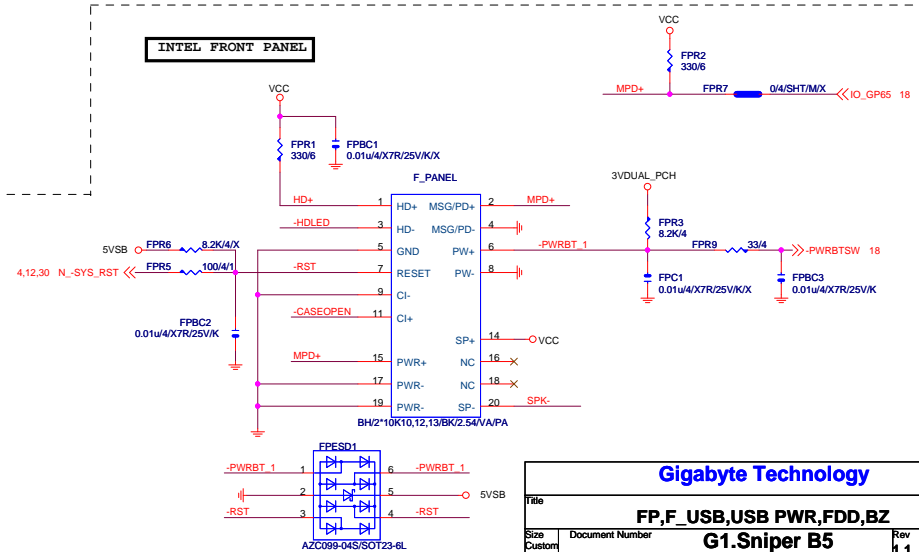
SATA LED



## SPKR

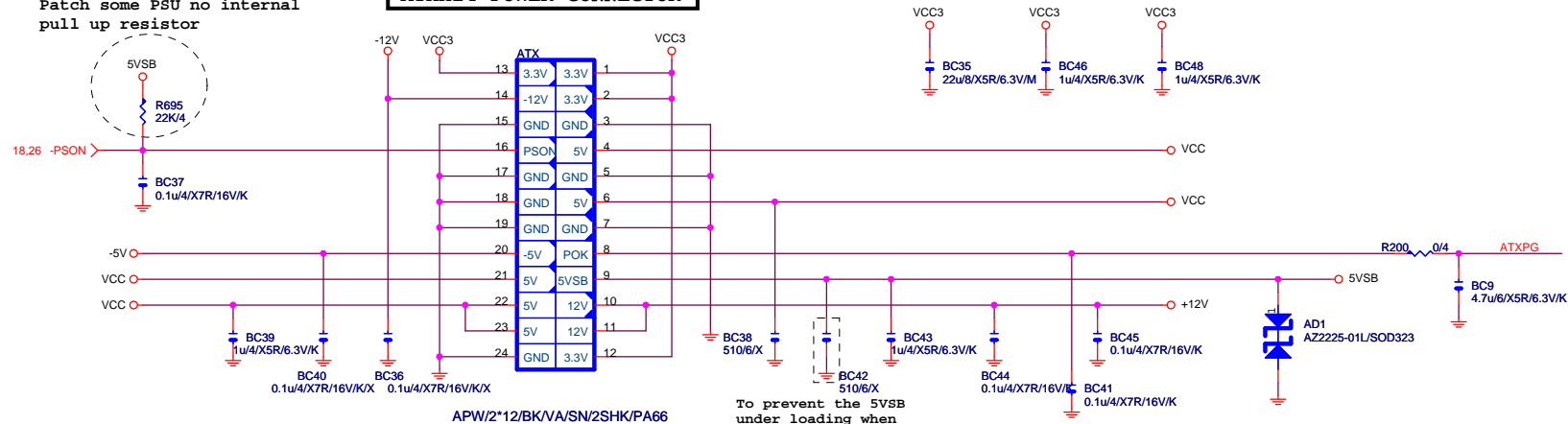


## INTEL FRONT PANEL

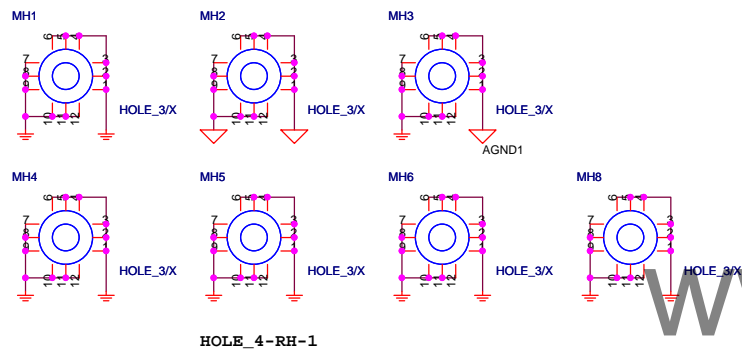
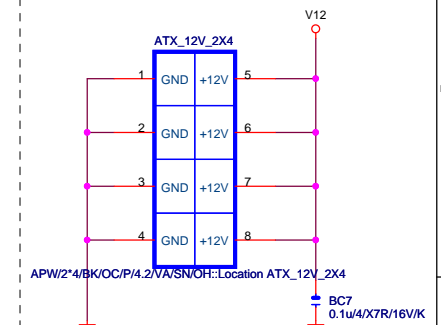


Patch some PSU no internal pull up resistor

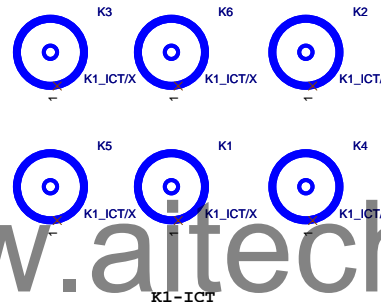
## ATXX24 POWER CONNECTOR



## ATXX4 POWER CONNECTOR

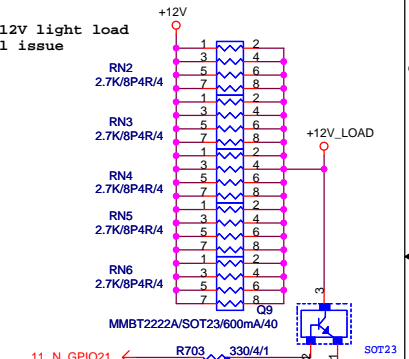


To prevent the 5VSB under loading when boot



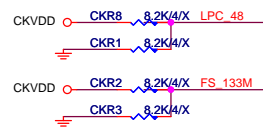
## 【技術通報R&D技術通報153】

To fix 12V light load abnormal issue

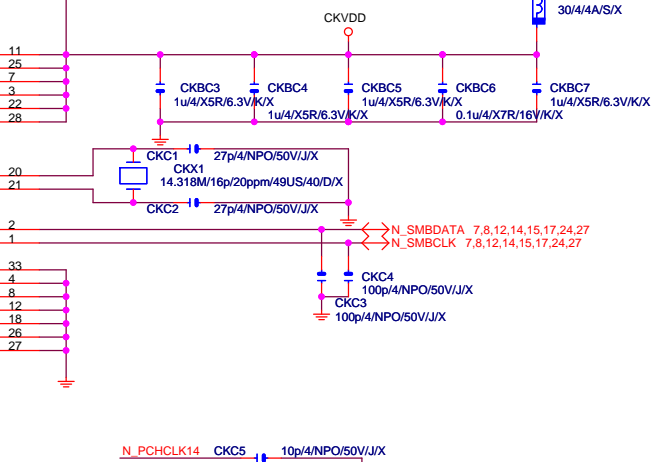
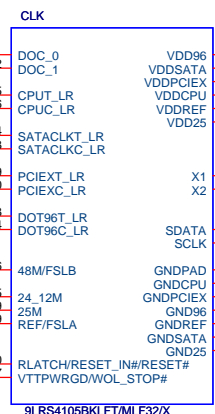
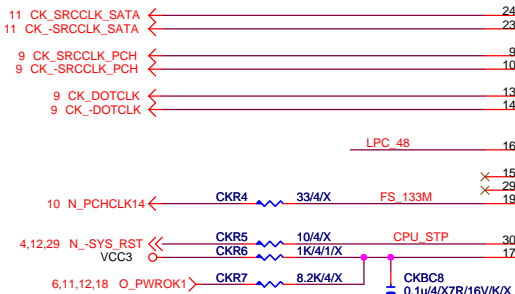


## CLK GEN

### CPU Frequency Selection

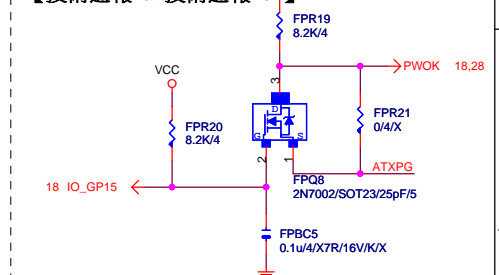


FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



## PWOK PATCH

### 【技術通報R&D技術通報154】



## Gigabyte Technology

Title			ATX POWER CONNECTOR		
Size	Document Number	G1.Sniper B5			Rev
Custom					1.1
Date:	Thursday, June 27, 2013	Sheet	30	of	34

[illegible]

The division voltage of VIN2 & VIN3 must be around 2.9V

Figure 10 is a schematic diagram of the 180p/8P4C/6/NPO/50V/K CN1 connector. It shows the connection of signals KDAT, KCLK, MDAT, and MCLK to pins 1 through 4 of the connector. The signals are connected to pins 1, 2, 3, and 4 respectively. The FUSEVCC\_R7 is connected to pin 5 and AGND1 is connected to pin 6. The connector is labeled 180p/8P4C/6/NPO/50V/K.

ART FAN

VCC

8.2K/4

18 FANPWM1

SYS FAN\_3

100/4/1

+12V

R673 3.3K/4/1

R677

R678 6.2K/4/1

C234 0.047u/4/X7R/16V/K

FANIO1 18

SHORT PROTECT

R0402-2

C233 1u/6/X7R/16V/K

EC11 100u/OS/D/16V/69/A/35m

BC50 0.1u/4/X7R/16V/K

CPU\_FAN FAN1\*4/BK/A3/PA66

Anti Spike

**SYS\_FAN\_1**      **Linear SYS\_FAN2V**

[illegible]

**SYS\_FAN\_3** **Linear SYS\_FAN**

18 FANPWM4

VCC3

R688 1K/4

R693 22K/4

BC219 1u4/X5R/6.3V/K

R689 8.2K/4

R690 8.2K/4

LM358DR/SO8

Q84 P2003ED/P/T0252/30m

R691 0/4/X

R692 8.2K/4

R8 3.3K/4/1

R7 15K/4/1

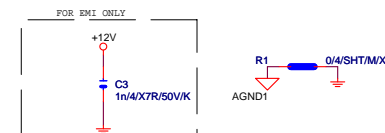
R6 6.2K/4/1

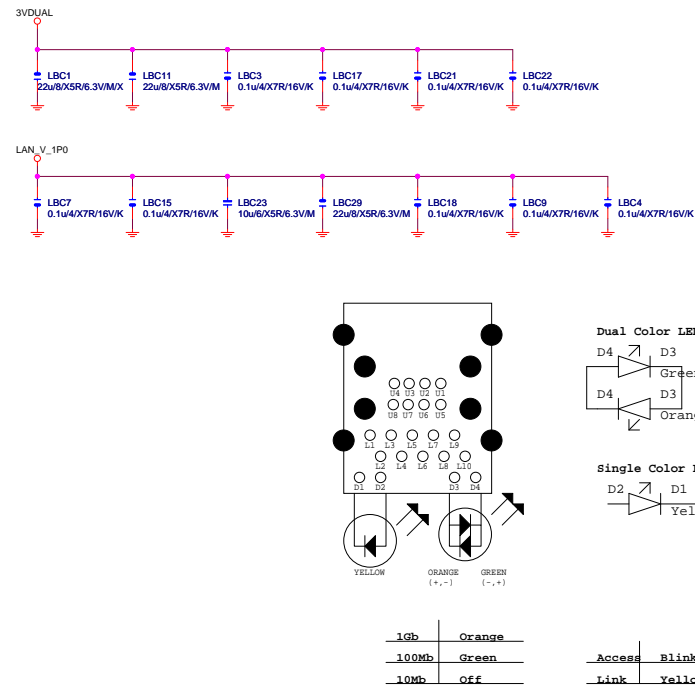
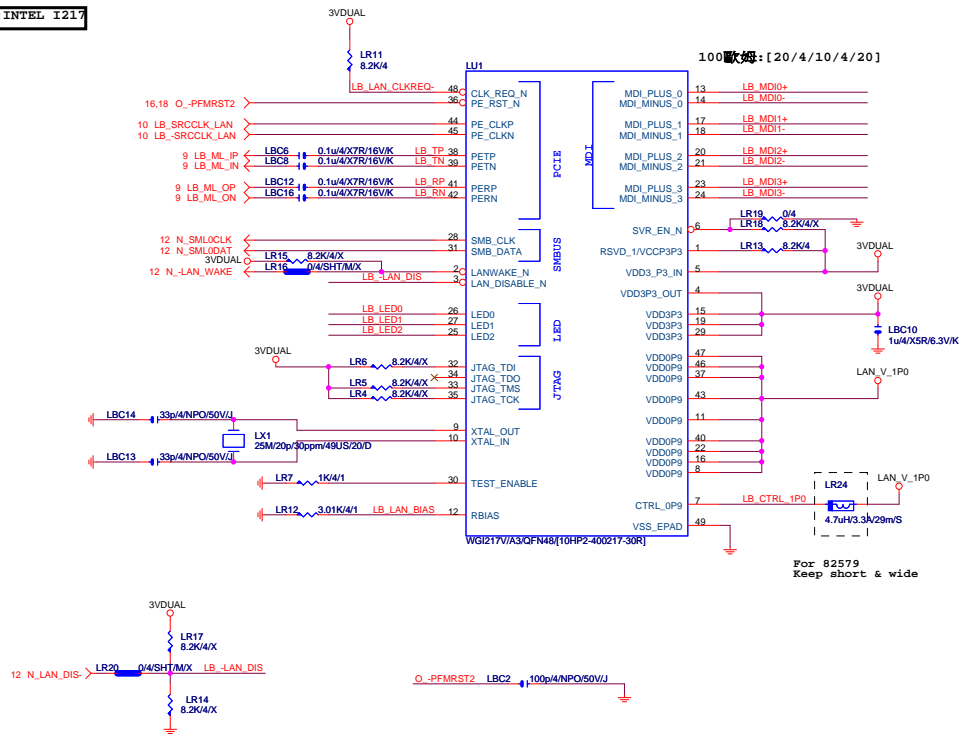
C2 0.047u4/X7R/16V/K

FANIO4 18

EC10 100uOS/D/16V/69/35m

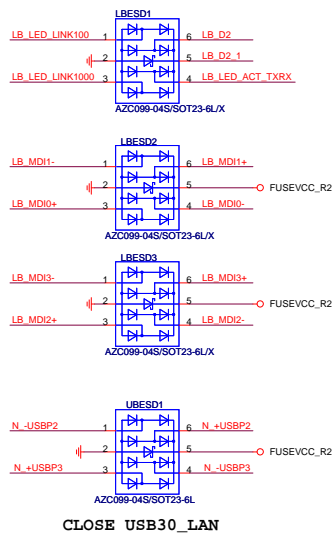
BC53 FAN/1\*/4BK/3PA66 0.1u4/X7R/16V/K



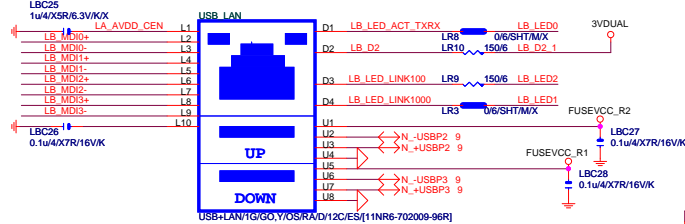


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100 歐姆: [20/4/10/4/20]

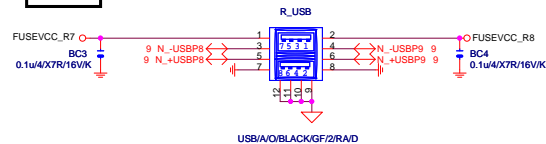


CLOSE USB30\_LAN

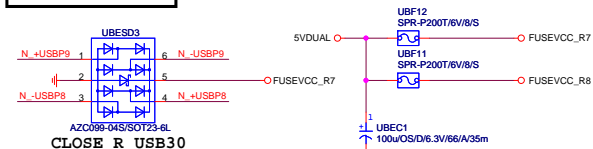


90 歐姆: [15/4.5/7.5/4.5/15]

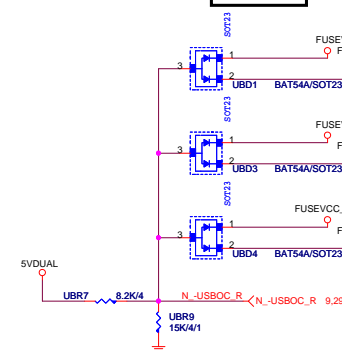
R\_USB30



USB20 ESD PROTECT



-USBOC\_R

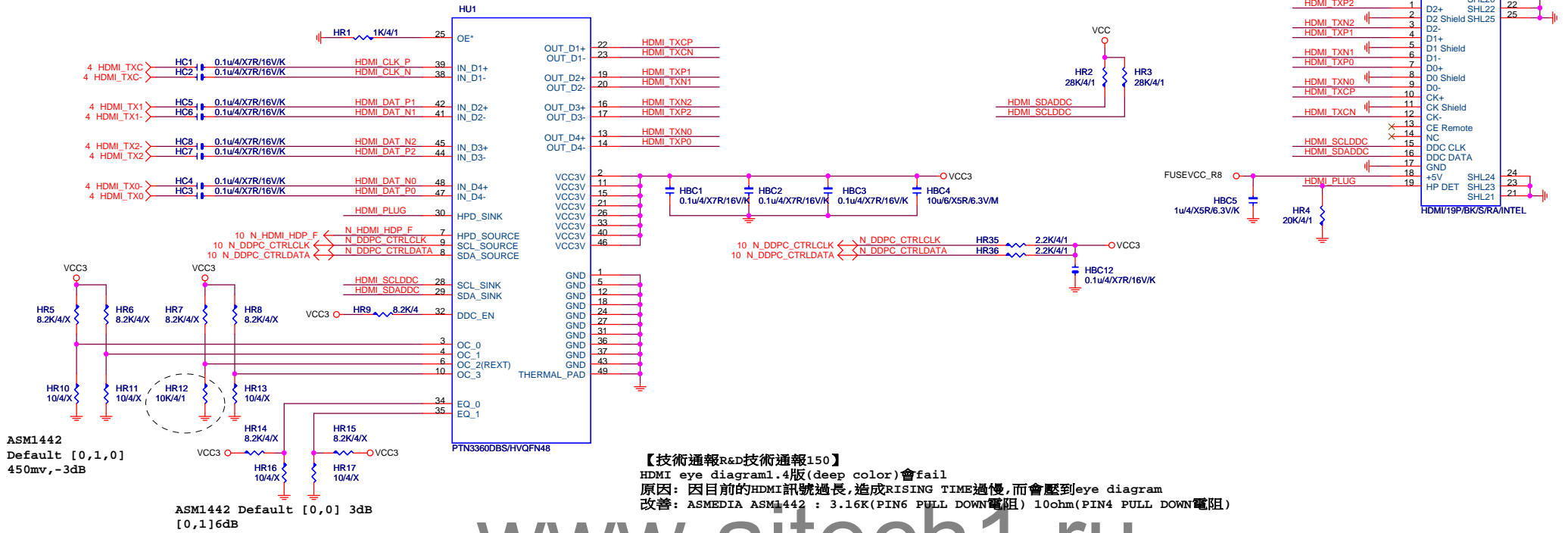




## HDMI LEVEL SHIFT

HDMI: 20/4/6/4/20

Impedance=85 +- 17.5%



【技術通報R&amp;D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

原因：因目前的HDMI訊號過長，造成RISING TIME過慢，而會壓到eye diagram

改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

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**GIGABYTE™**

Title	<b>HDMI</b>
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Size	Document Number
Custom	

## G1.Sniper B5

## 1.1

Date: Thursday, June 27, 2013

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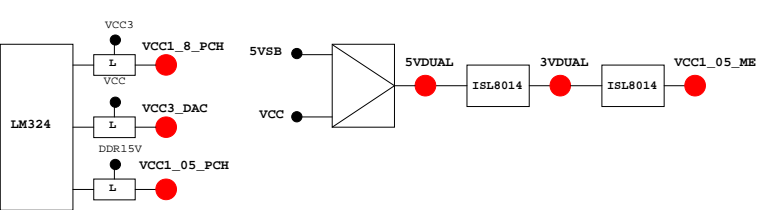
PCH GPIO LIST TABLE

PIN NAME	PWR	Default	USAG	NOTE
GP0	MAIN	H-Z	GPIO0	N/A
GP1/TACH1	MAIN	GPI	GPIO1	N/A
GP2/PIRQE#	MAIN	GPI	~PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	GPI	~PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	GPI	~PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	GPI	~PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN	GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8
GP9/OC5#	STBY	NATIVE	USB OC5#	N/A
GP10/OC6#	STBY	NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY	NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12
GP13	STBY	L	GPI	LPCPME#
GP14/OC7#	STBY	NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)
GP16	MAIN	GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN	GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN	GPI	Mobile Only	N/A
GP19	MAIN	GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN	GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN	GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22
GP23	MAIN	GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#
GP25	STBY		Mobile Only	N/A
GP26	STBY		Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27
GP28	STBY	H	GPO	PWR LED
GP29	STBY	L	GPI	GPIO29
GP30	STBY	H-Z	GPI	Mobile Only
GP31	STBY	H-Z	GPI	Mobile Only
GP32	MAIN	H	GPO	N/A
GP33	MAIN	H	GPO	N/A
GP34	MAIN	H-Z	GPI	~PCI_STOP
GP35	MAIN	L	GPO	~ACZ_DET
GP36	MAIN	GPI	N/A	N/A
GP37	MAIN	GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect
GP39	MAIN	H-Z	GPI	GPIO39
GP40	STBY	NATIVE	USB OC1#	N/A
GP41	STBY	NATIVE	USB OC2#	N/A
GP42	STBY	NATIVE	USB OC3#	N/A
GP43	STBY	NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44
GP45	STBY	NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46
GP47	STBY		Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48
GP49	MAIN	H-Z	IN	GPIO49
GP50	MAIN	NATIVE	~REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	~GNT1
GP52	MAIN	NATIVE	~REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	~GNT2
GP54	MAIN	NATIVE	~REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	~GNT3
GP56	STBY	NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1
GP58	STBY	H-Z	NATIVE	F_USB_OC
GP59	STBY	NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)
GP61	STBY	L	NATIVE	~SUSTAT
GP62	STBY	L	NATIVE	SUSCLK
GP63	STBY	L	NATIVE	GPIO63
GP64	MAIN	L	NATIVE	CLKOUTFLEX0
GP65	MAIN	L	NATIVE	CLKOUTFLEX1
GP66	MAIN	L	NATIVE	CLKOUTFLEX2
GP67	MAIN	L	NATIVE	CLKOUTFLEX3
GP72	STBY	H-Z	NATIVE	VCORE_OV4
GP73	STBY		Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2
GP75	STBY	H-Z	NATIVE	N/A(Reverse)

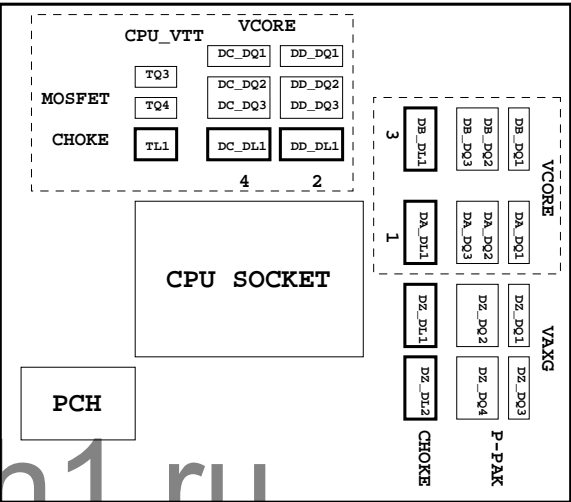
Super I/O ITE8720 GPIO Table

PIN NAME	USAG	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAG	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SEN	LOW_PWR_1	
VIDO5/GP27/SEN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

散熱模組料號:

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
TABLE LIST			
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Date:	Thursday, June 27, 2013	Sheet	34 of 34